14 Semiconductor Electronics: Materials, Devices and Simple Circuits

Facts that Matter

• Classification of Metals, Conductors and Semiconductors

On the basis of the relative values of electrical conductivity (σ) or resistivity (ρ), the solids are broadly classified as follows:

(*i*) **Metals:** They possess high conductivity and low resistivity. The resistivity of these materials range from 10^{-2} Ω m to 10^{-8} Ω m and the value of conductivity for such materials lie between 10^{2} to 10^{8} S m^{-1}. For example: Ag, Au, Cu, Al, etc.

(*ii*) **Insulators:** They have very high resistivity and very low conductivity. The value of resistivity for these materials lie between 10^{11} to 10^{19} Ω m while the conductivity range is 10^{-11} to 10^{-19} S m^{-1}. For example: rubber, plastic etc.

(*iii*) **Semiconductors:** They have resistivity and conductivity between metals and insulators. The value of resistivity for semiconductors lie between 10^{-5} to 10^{6} Ω m whereas conductivity lies between 10^{5} to 10^{-6} S m^{-1}.

Further, semiconductors can be classified in the following manner:

(*a*) **Elemental semiconductors:** The semiconductors which are available in natural form. For example: Silicon (*Si*) and Germanium (*Ge*).

(*b*) **Compound semiconductors:** By compounding the metals, these semiconductors are made. Examples are:

- Inorganic: CdS, GaAs, CdSe, InP, etc.
- Organic: anthracene, doped pthalocyanines, etc.
- Organic polymers: polypyrrole, polyaniline, polythiophene, etc.

• Energy Bands of Solids

In the bond description of solids the bonding electrons and holes have been considered as highly localised, which is not exact due to strong overlapping of the orbitals, alternative approach is termed as energy band description of solids. The electron energies in solids, in view of strong overlap of different atomic orbitals, will be more like an energy band instead of discrete energy levels of single isolated atoms.

In crystal, the atoms are close to each other and therefore, the electrons interact with each other also with the neighbouring atomic cores. The overlap or interaction will be more felt by the electrons in the outermost orbit while the inner orbit or core electron energies may remain unaffected.

When these atoms start coming nearer to each other to form a solid. The total number of available

energy states 8N has been re-apportioned between the two bonds (4N states each in the lower and upper energy bands). Here the significant point is that there are exactly as many states in the lower band (4N) as there are available valence electrons from the atom (4N).

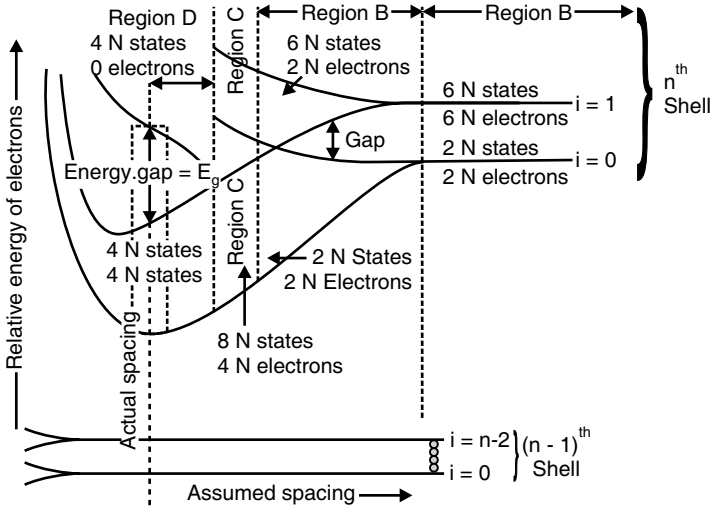


Fig. 14.1

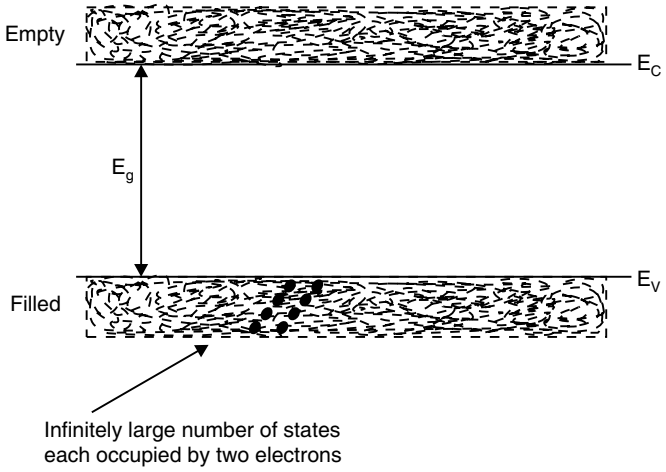


Fig. 14.2

The collection of very closely spaced energy levels is called an energy band. The band of filled energy levels is called the valence band and the band of unfilled energy levels is called the conduction band. Generally, the valence band and the conduction band are separated by a gap called the forbidden band or the energy band gap (energy gap). It is the width of the energy gap which decides whether a solid is a semiconductor, an insulator or a conductor.

In case of metal, bands are overlapping $E_g = 0$. For insulator large band gap E_g exists ($E_g > 3$ eV). In case of semiconductor, finite but small band gap ($E < 3$ eV).

An intrinsic semiconductor will behave like an insulator at $T = 0K$. It is the thermal energy at high temperature ($T > 0K$) which excites some electrons from the valence band (thus creating an equal number of holes in the valence band) to the conduction band.

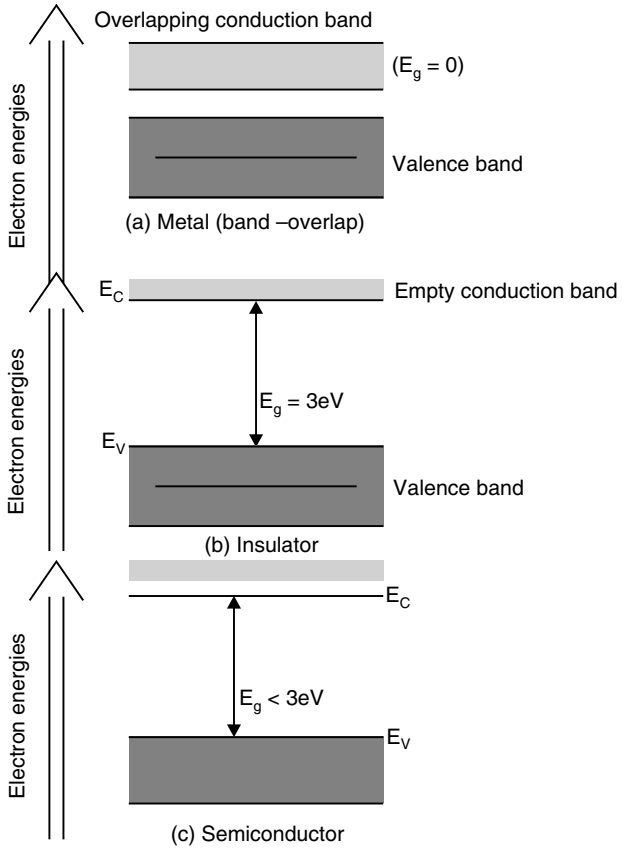
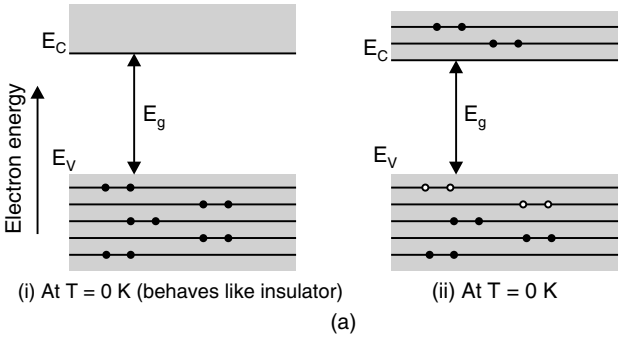


Fig. 14.3

In case of extrinsic semiconductors, additional energy states, apart from E_C and E_V due to donor impurities (E_D) and acceptor impurities (E_A) also exist. We know that very small energy (~0.1eV) is required for the electrons to be released from the donor impurity in the *n*-type semiconductor. Hence, the donor energy E_D lies very near the bottom of the conduction band.



Energy band diagrams, description is grossly approximate and hypothetical. It helps in understanding the difference between metals, insulators and semiconductors in a simple manner.

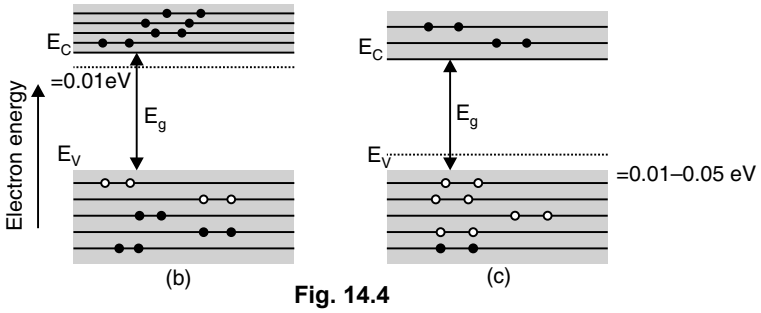


Fig. 14.4

• Intrinsic Semiconductor

The pure semiconductors in which the electrical conductivity is totally governed by the electrons excited from the valence band to the conduction band and in which no impurity atoms are added to increase their conductivity are called intrinsic semiconductors and their conductivity are called intrinsic conductivity.

From diagram, it is clear that the number of electrons so generated will be equal to the number of holes. Hence, in intrinsic semiconductors,

$$n_e = n_h = n_i$$

where, n_e, n_h and n_i represent the number of free electrons, holes and number of overall charge carriers present. If I_e and I_h represent the current due to electrons and holes respectively, then the total current

$$I = I_e + I_h$$

Demerits of intrinsic semiconductor:

- Have very small number of charge carriers (10^{-16} m^{-3}) hence a low conductivity.
- Need to be thermally agitated in order to knock off electrons and generate holes.
- Have equal number of carriers of both types, *i.e.*, $n_e = n_h$.

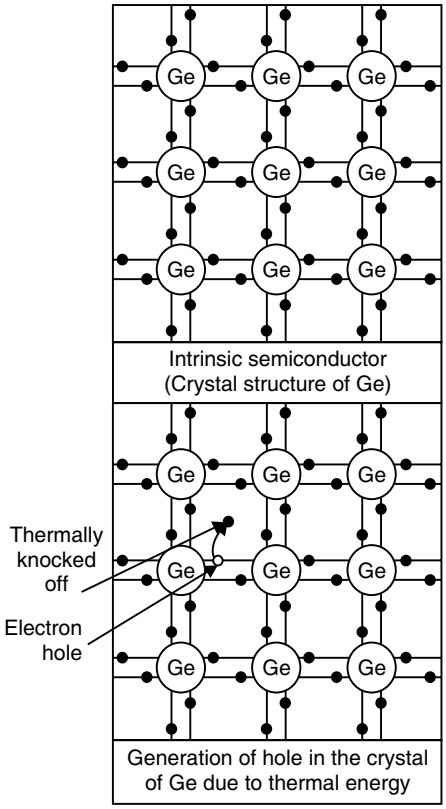


Fig. 14.5

• Extrinsic Semiconductors

A semiconductor doped with suitable impurity atoms so as to increase its conductivity is called an extrinsic semiconductor Extrinsic semiconductors are of two types:

(*i*) *n*-type semiconductors

(*ii*) *p*-type semiconductors

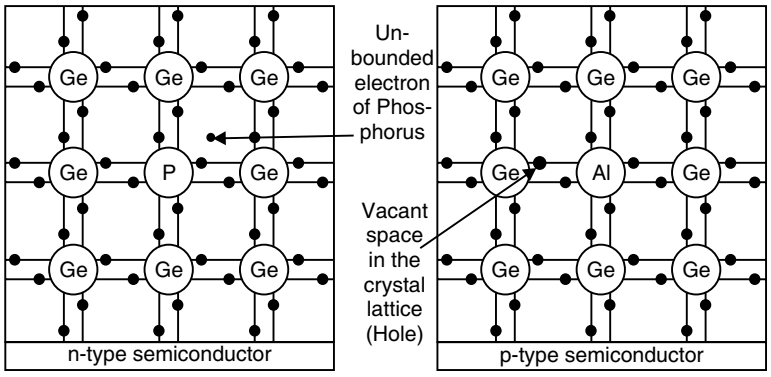


Fig. 14.6

(*i*) *n*-type Semiconductors: The pentavalent impurity atoms are called donors because they donate electrons to the host crystal and the semiconductor doped with donors is called *n*-type semiconductor. In *n*-type semiconductors, electrons are the majority charge carriers and holes are the minority charge carriers. Thus,

$$n_e \cong n_d >> n_h$$

(*ii*) *p*-type Semiconductors: The trivalent impurity atoms are called acceptors because they create holes which can accept electrons from the nearby bonds. A semiconductor doped with acceptor type impurities is called a *p*-type semiconductor. In *p*-type semiconductor, holes are the majority carriers and electrons are the minority charge carriers. Thus,

$$N_a \cong n_h >> n_e$$

• Distinction between Intrinsic and Extrinsic Semiconductor

1. Intrinsic semiconductors are pure Group IV elements whereas extrinsic semiconductors have some impurity in the form of Group V or Group III elements externally introduced in the pure semiconductors.
2. In intrinsic semiconductors, the conductivity is only slight; but due to the added impurity, the extrinsic semiconductors have a greatly increased electrical conductivity.
3. In intrinsic semiconductors, the conductivity increases with the rise in temperature; while in extrinsic semiconductors, the value of conductivity depends upon the amount of impurity added to the semiconductor.
4. In intrinsic semiconductor, the number of holes is always equal to the number of electrons; while this is not the case in extrinsic semiconductors. In *n*-type, the number of electrons is much greater than the number of holes; and in *p*-type, the number of holes is much greater than the number of electrons in it.

The vacancy or absence of electron in the bond of a covalently bonded crystal is called a hole. A hole serves as a positive charge carrier.

• Conductivity of Semiconductors

When a potential difference $v = El$ is applied across a semiconductor of length l and area of cross-section A, the electrons being negative charge particles move from lower potential to higher potential and the holes being positive charged particle move from higher potential to lower potential constituting current in the same direction as the current of electrons. Therefore, the net current in the semiconductor from higher potential to lower potential,

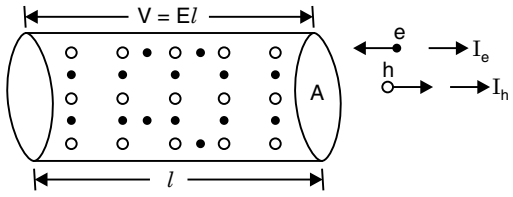


Fig. 14.7

$$I = I_e + I_h$$

where, $I_e = neAv_e(e)$ is the current-due to electrons, n_e = number density of free electrons and v_e is the drift speed free electrons. And $I_h = n_h Av_h(e)$ is the current due to holes, n_h = number density of holes and v_h is the drift speed of holes.

$\because$ $$I = \frac{V}{R}$$

$\therefore$ $$\frac{V}{R} = n_e eAv_e + n_h eAv_h$$

or $$\frac{El}{\rho \frac{l}{A}} = n_e eAv_e + n_h cAv_h$$

or $$\frac{1}{\rho} = e\left[n_e \frac{v_e}{E} + n_h \frac{v_h}{E}\right]$$

or $$\boxed{\sigma = e\,[n_e \mu_e + n_h \mu_h]}$$

Where, $\sigma = \frac{1}{\rho}$ is the conductivity,

μ_e = the drift speed per unit electric field *i.e.,* mobility of free electron, and

μ_h = mobility of holes.

• Mass Action Law

Doping with *N*-type impurities decreases the number of holes and doping with *P*-type impurities decreases the concentration of free electrons as compared to intrinsic semiconductors.

In an *intrinsic semiconductor* the number of holes and electrons is equal. Hole-electron pairs continue disappear as a result of recombination whereas new electron-hole pairs are produced due to thermal agitation. But number density of electrons and holes remain same

$$n_e = n_h = n_i$$

where n_i is called intrinsic concentration. Under thermal equilibrium the product of free negative and positive concentrations is a constant. It is independent of doner and accepter impurities doping. This is called the mass action law and is given by

$$n_e \times n_h = n_i^2$$

However, intrinsic concentration is a function of temperature.

• Electrical Neutrality

If there are N_D donor atom, they are all in ionised state; the positive charge density is $N_D + n_h$. Similarly total negative charge density is $N_A + n_e$, where N_A is concentration of acceptor impurity. According to electrical neutrality of semiconductor,

$$N_D + n_h = N_A + n_e \quad ...(i)$$

For *N*-type material, $N_A = 0$ and $n_e >> n_h$ which leads to

$$n_e = N_D \quad ...(ii)$$

Hence in *N*-type material free electron concentration is approximately equal to the density of donor atoms (N_D is concentration of donor atom).

Similarly *P*-type material $n_h >> n_e$ and $N_D = 0$ which leads to

$$n_h = N_A \quad ...(iii)$$

from mass action law

$$n_e \,.\, n_h = n_i^2 \quad ...(iv)$$

Thus, for *N*-type semiconductor

$$n_h = \frac{n_i^2}{N_D} \quad ...(v)$$

and for *P*-type semiconductor

$$n_e = \frac{N_e^2}{N_A} \quad ...(vi)$$

- The density of a hole-electron pair increases with temperature. As a result conductivity increases. The intrisic concentration n_i varies with temperature T as

  $$n_i = A_0 T^3 e^{-E_g/KT}$$

  where E_g is the forbidden energy gap at zero kelvin in electron volt, K is Boltzmann's constant in eV/k and A_0 is constant.

- With a rise in temperature there are increased thermal lattice vibrations due to which resistance increases. But in case of semiconductors the number of charge carriers vary rapidly with rise in temperature. The overall effect is increased in conductivity of semiconductor
- Experimentally it has been found that the forbidden energy gap E_g depends on temperature.

  For silicon semiconductor

  $$E_g(T) = 1.21 - 3.60 \times 10^{-4}\ T.$$

  For germanium semiconductor

  $$E_g(T) = 0.785 - 2.23 \times 10^{-4}\ T$$

  At room temperature (300 K),

  For silicon, $E_g = 1.1$ eV

  For germanium, $E_g = 0.72$ eV

  Adding equal concentration of donor and acceptor atoms to *P*-type and *N*-type semiconductor respectively results in an intrinsic semiconductor when concentration of donor atoms exceeds the acceptor concentration in a *P*-type semiconductor, it is changed from a *P*-type to an *N*-type semiconductor.

• *p-n* Junction

It forms the basic unit of a semiconductor device and is referred to as diode. There are many techniques used for creating such junction diodes, as per requirements.

***p-n* Junction without Applied Voltage (No Bias):**
(Figure 14.8)

When a *p*-type semiconductor is effectively combined with an *n*-type semiconductor, the holes from *p*-type diffuse into *n*-type and electrons from *n*-type diffuse into *p*-type semiconductor. Thus, recombination of these charge carriers occurs near the junction causing the depletion layer formation. On the *n*-side of the depletion layer, there are effective *+ve* charges and on the *p*-side, there are effective *–ve* charges. Thus, a potential difference develops across this layer, which prevents further diffusion of charge carriers. Hence, it acts as a barrier and is known as barrier potential (V_B). The energy difference across the depletion layer will be qV_B, where q is the charge crossing the barrier. Depletion layer width (junction width) and the potential barrier depend upon the doping concentration. If number of acceptors (in *p*-type) (N_A) and number of donors (in *n*-type) (N_D) are small, the electrons and the holes can diffuse upto a longer distance and hence the width of the depletion layer will be large and the potential across the barrier will be small.

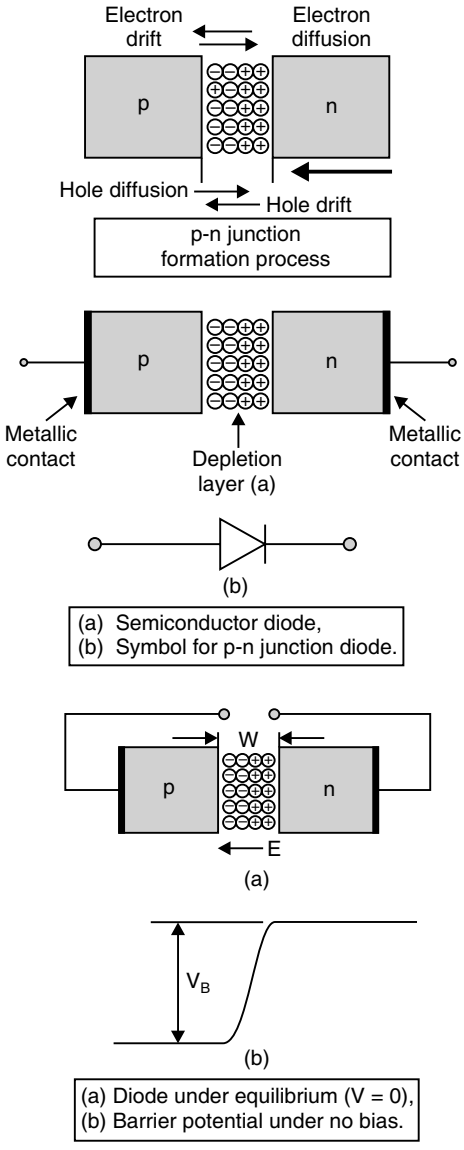


Fig. 14.8

***p-n* Junction with Applied Voltage (or Bias):**(figure 14.9)

Forward Bias: When applied voltage is such that *n*-side is negative and *p*-side is positive, the applied voltage is opposite to the barrier potential. Hence,

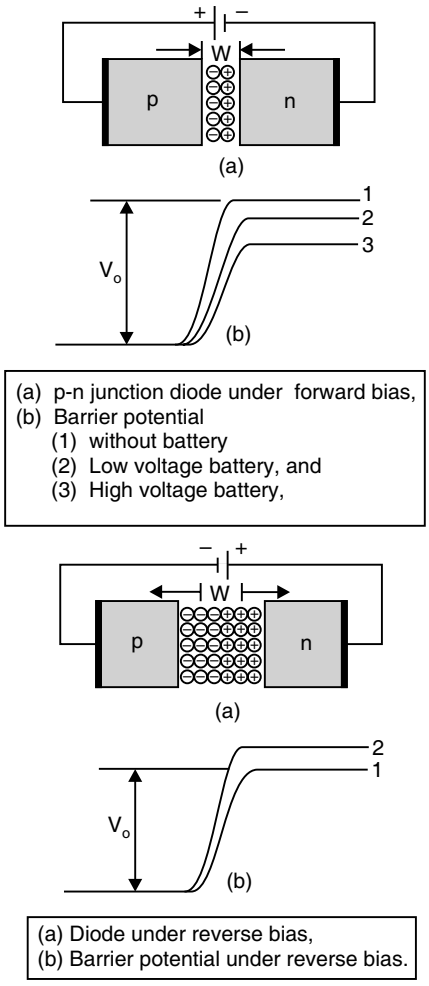
1. The effective barrier potential becomes $V_B - V$, and the energy barrier across the junction decreases.
2. The majority carriers are allowed to cross the barrier, hence current is primarily due to majority carriers.
3. The junction width decreases.

The condition is known as forward bias, and the current flow in this bias is large (~*mA*).

Reverse Bias: When applied voltage is such that *p*-side is negative and *n*-side is positive, the applied voltage is in the direction of the barrier potential. Hence,

1. The effective barrier potential becomes $V_B + V$, and the energy barrier across the junction increases.
2. The minority carriers are allowed to cross the barrier, hence current is primarily due to minority carriers.
3. The junction width increases.

The condition is known as reverse bias, and the current flow in this bias is very small (~ μ*A*).



(a) p-n junction diode under forward bias,
(b) Barrier potential
(1) without battery
(2) Low voltage battery, and
(3) High voltage battery,

(a) Diode under reverse bias,
(b) Barrier potential under reverse bias.

Fig. 14.9

• Characteristics of *p-n* Junction Diode

Forward: It is a graphical relation between the forward bias applied and the forward current flowing through the diode. As long as the forward bias is less than the barrier potential, no current flows. But when a forward bias is greater than barrier potential applied, an almost linear forward current (≈ a few *mA*) flows due to the flow of majority carriers.

Reverse: It is a graphical relation between the reverse bias applied and the reverse current flowing (if any). In this case, the majority carriers in *p* and *n*-type both move away from the junction so that no majority current flows. However, minority carriers do cross over the junction constituting a small current (≈ a few μ*A*) which is called minority current or leakage current. As the magnitude of the reverse bias is increased (in magnitude), the leakage current also rises gradually. At a particular reverse bias, the reverse current increases abruptly (*i.e.,* it becomes very large suddenly). The reverse bias at which the reserve current rises abruptly, is called Zener voltage or Breakdown voltage.

• Application of *p-n* Diode as a Rectifier

As shown in figure 14.10, the secondary of the transformer supplies the desired *ac* voltage across *A* and *B*. When the voltage *A* is positive, the diode conducts, when *A* is negative, the diode is reverse biased and it does not conduct and we get an output voltage as shown in figure 14.11.

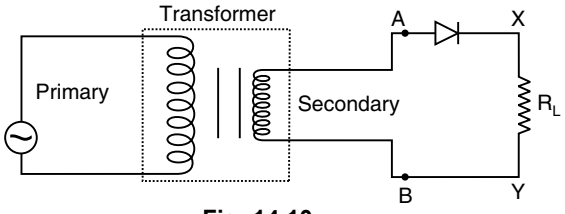


Fig. 14.10

The output voltage, though still varying is restricted to only one direction and is said to be rectified. This circuit is known as **half wave rectifier** because only half cycle we get a voltage in the output.

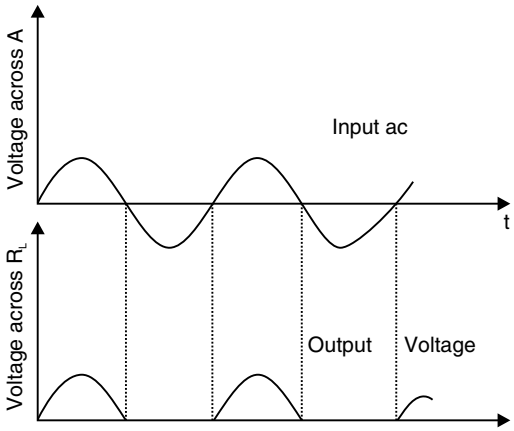


Fig. 14.11

Full Wave Rectifier: Using two diodes, shown in figure gives rectified output voltage corresponding to the positive as well as negative half of the *ac* cycle. The secondary of the transformer is wound into two equal parts. The voltage at any instant at *A* (input of diode D_1) and *B* (input of diode D_2) with respect to the centre tap are out of phase with each other because of that we get output voltage during the +*ve* as well as the –*ve* half of cycle (during the full wave). Therefore this circuit is known as full wave rectifier.

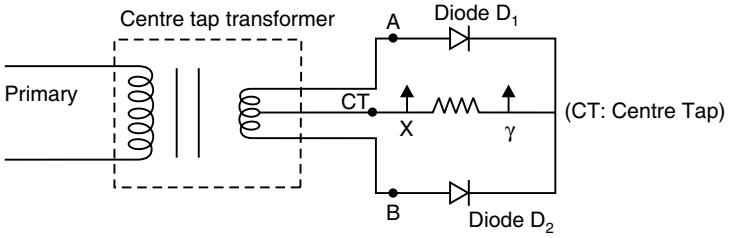


Fig. 14.12

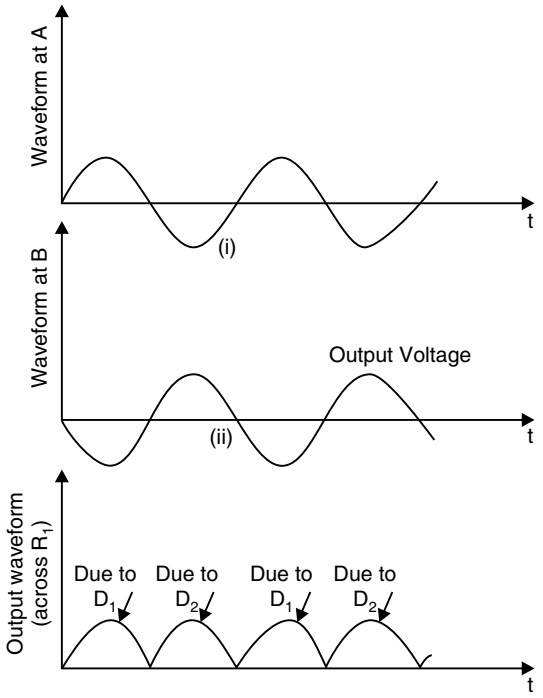


Fig. 14.13

The rectified voltage is still varying voltage but restricted to only one direction. From this rectified voltage, we can obtain *dc* voltage by filtering out the *ac* components. In general, a high value of *c* provide a low impedance path *ac* but high, almost infinite impedance to *dc* $\left(X_c = \frac{1}{\omega C}\right)$. Hence, *ac* is by passed through *c* or filtered. *DC* like voltage appears at the load.

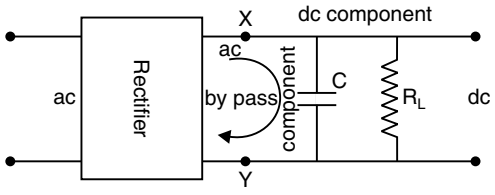


Fig. 14.14

• Zener Diode

Zener diode is a highly doped junction diode having very thin depletion layer. As V–I characteristics shown in Fig. 14.15. There is a point where further increase of negative voltage results in a sharp increase in current. This voltage is called zener voltage (V_z).

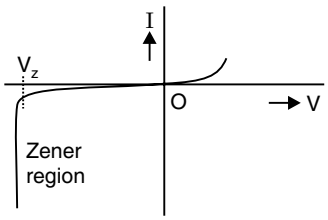


Fig. 14.15

When the voltage across diode is increased in the reverse bias region, the minority carriers gain velocity and associated kinetic energy. These minority carriers are responsible for the reverse saturation current. The collision of these minority charge carriers with atomic structure will result in an ionisation process. The valance electrons absorb sufficient energy in these collisions and leave the parent atom. These additional carriers help the ionisation process and a very high current is established. This current is called *avalanche current* and the region in which this current is established is called *avalanche breakdown* region. The magnitude of Zener voltage may decreased by increasing doping levels in the *P*-type and *N*-type region of junction diode.

When the Zener voltage (V_z) decreases to a very low level, there is a strong electric field in the region of the junction that can break the bonds within the atom and generate change carriers. The mechanism is called *Zener break down*. Zener break down is significant only at lower value of V_z. The diodes which works in the Zener region of characteristic are called *Zener diodes* The maximum reverse-bias voltage that can be applied before commencement of Zener region is called peak inverse voltage (P/V)

• Zener Diode as Voltage Regulator

When the ac input voltage of a rectifier fluctuates, its rectified output also fluctuates. To get a constant dc voltage from the dc unregulated output of a rectifier Zener diode is used the circuit diagram is shown in Fig. 14.16.

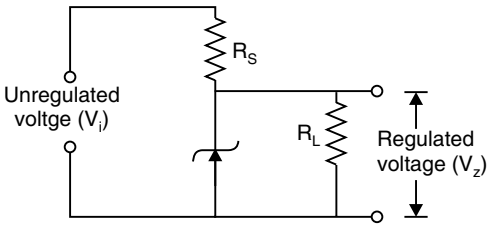


Fig. 14.16

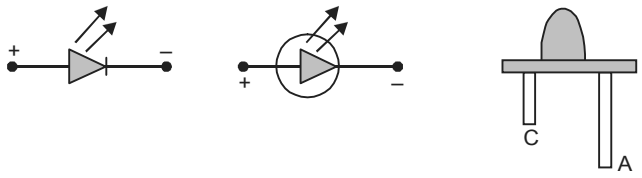
The unregulated dc voltage is connected to the Zener diode through a series resistance R_S such that the Zener diode is reverse biased. If the input voltage increases, the current through and Zener diode increases. This increases the voltage drop across R_s without any change in the voltage across Zener diode. This is because in the break down region Zener voltage remains constant even through the current through the Zener diode changes.

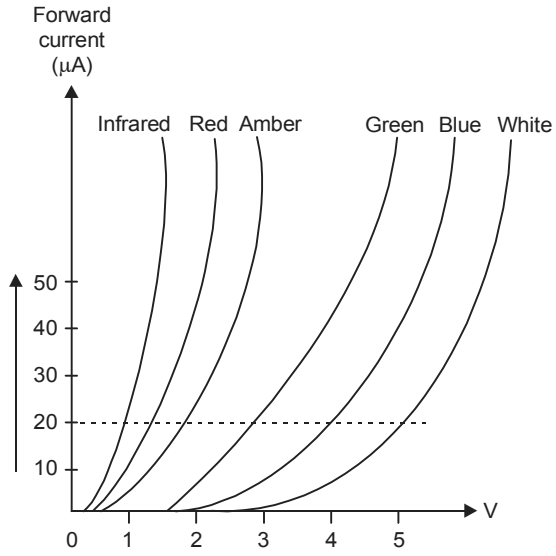
Similarly, if the input voltage decreases, the current through R_s and Zener diode also decreases. The voltage drop across R_s, decreases without any change in the voltage across the Zener diode. Thus any increase/decrease in the input voltage results in, increase/decrease of the voltage drop across R_s without any decrease of the voltage drop Zener diode. Thus the Zener diode acts as a voltage regulator.

- **Light Emitting Diode (LED)**

It is a heavily doped *p-n* junction which under forward bias emits spontaneous radiation. When a conduction electron makes a transition to valance band to fill up a hole in *P-N* junction the extra energy may be emitted as a photon lies is the visible range, LED are made of semiconductor materials like gallium arsenide or indium phosphide. These are used in electronic gadgets as indicator lights.

- **LED Symbol and Shape**





LED is usually used as low voltage DC supply for their operation. A given LED has a safe value of the forward current that it can carry. This value is around 5 mA for the usual simple LEDs and can go up to 30 mA or more for LEDs needed for providing a high brightness output light. In practice, it is usual to have a suitable senses resistor connected to the LED, so that the forward current is limited to within its safe value.

The V-I characteristics of a LED is similar to that of a Si junction diode. But the threshold voltages are much higher and slightly different for each colour. The reverse breakdown voltages of LEDs are very low, typically around 5 V. The LEDs find extensive use in remote controls, burglar alarm systems, optical communication, etc.

- **Solar Cell**

In solar cell an electron in the valance band may absorb photon and be promoted to conduction band, leaving a hole behind devices in which light generated electrons and holes are separated by a junction field are called *solar cell or photo voltatic devices*.

- **Photodiode**

It is a junction diode which operated under reverse bias but less than breakdown voltage. When the photo diode is illuminated with light having energy greater than the energy gap of the semiconductor, then electron-hole pairs are generated due to the absorption of photons. The diode is fabricated such that the generation of electron hole pairs takes place in or near the depletion layer region of the diode. Due to electric field of the junction, electron and holes are separated before they recombine. The direction of the electric field is such that electrons reach *n*-side and holes reach *p*-side. Electrons are collected on *n*-side and holes are collected on *p*-side giving rise to an emf.

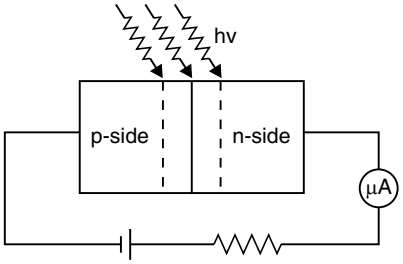


Fig. 14.17

Photodiode can be used as a photo detector to defect optical signals. The circuit diagram used for the measurement of *I-V* characteristics of a photodiode is shown in Fig. 14.17 and a typical *I-V* characteristics for different intensities of light $I_1 < I_2 < I_3$ are shown in Fig. 14.18.

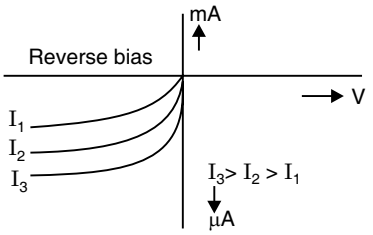


Fig. 14.18

- **Transistor**

It is a three-layer semiconductor device consisting of two *P*-type and one *N*-type. When *P*-type semiconductor is sandwiched between two *N*-type semiconductor, it is called *N-P-N* transistor. When *N*-type semiconductor is sandwiched between two *P*-type semiconductors, it is called *P-N-P* transistor.

Transfer of a current from a low resistance to a high resistance circuit produces the basic amplifying action of transistor. A combination of the words 'transfer' and 'resistance' give term transistor, *i.e.*,

Transfar + Resistor → Transistor

Transistor has three parts:

- **Emitter**

The emitter layer is highly doped and kept in forward bias. The charge carriers appear to emit from this region, hence called emitter.

- **Collector**

The collector layer is modraterly doped and kept in reverse bias. The charge carriers appear to be collected in the region, hence called collector.

- **Base**

The layer between emitter and collector is called base. The base is very lightly doped. The base-emitter junction is forward biased, offering low resistance to the emitter circuit. The base-collector junction is reverse biased offerening high resistance to the collector circuit.

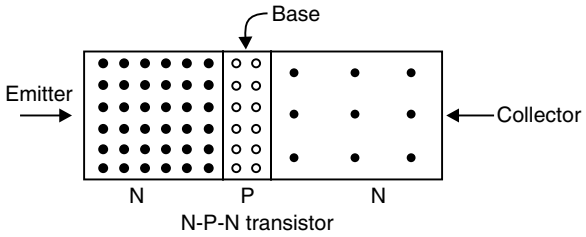


Fig. 14.19

The *P-N-P* transistor and *N-P-N* transistor are shown in Fig. 14.19 and 14.20.

- Due to forward bias a large current enters the emitter-base junction but most of it is diverted to adjacent reverse-biased base-collector junction and the current coming out of the base becomes a very small fraction of the current that entered the junction. If I_h and I_e be the current due to holes and electrons respectively, the emitter current $I_E = I_h + I_e$ and the base

current I_B << I_h + I_e because a major part of I_E goes to collector instead of coming out of the base terminal.

As shown in the Fig 14.21 the current entering into the emitter from outside is equal to the emitter current I_E. Similarly the current emerging from the base terminal is I_B and that from collector terminal is I_C, According to Kirchhoff's law the emitter current is the sum of collector current and base current.

$$I_E = I_B + I_C$$

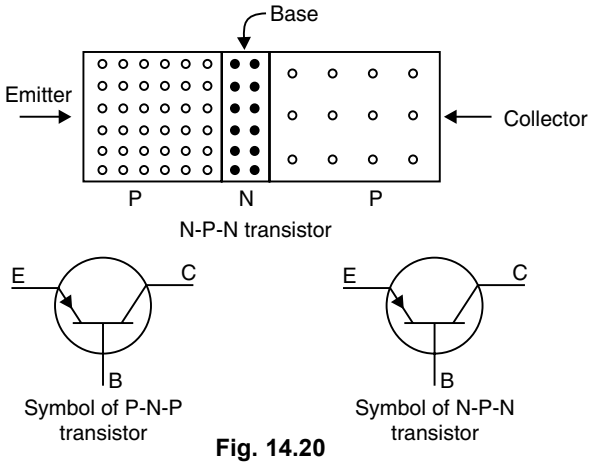


Fig. 14.20

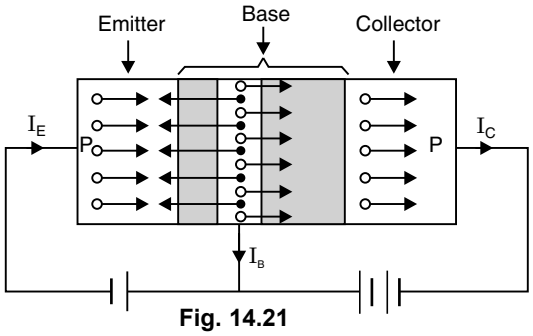


Fig. 14.21

• Common Emitter Transistor Characteristics

There are three types of characteristics of transistor (*i*) Input characteristics (*ii*) Output characteristics (*iii*) transfer or metal characteristics.

To study the characteristics of transistor the circuit diagram is made as shown in the Fig. 14.22.

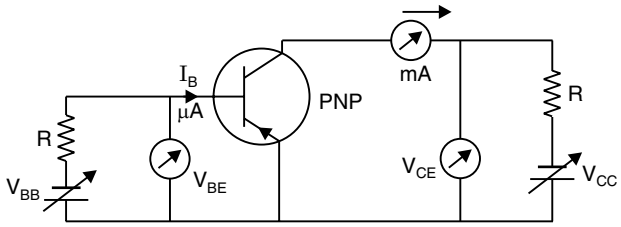


Fig. 14.22

To study the input characteristics of a transistor the change in input current (I_B) is observed with respect to change in input voltage (V_{BE}) at constant output voltage (V_{CE}).

To obtain the input characteristic when the transistor is in active state the collector-emitter voltage V_{CE} is kept constant and large enough to make the base-collector junction reverse biased. Since V_{CE} = V_{CB} + V_{BE} and for silicon transistor V_{BE} = 0.6 + 0.7 V. V_{CE} must be sufficiently larger than 0.7 *V*. The input characteristic may be obtained for a constant V_{CE} some where in the range of 3 *V* to 20 V. Since increase in V_{CE} appears as increase in V_{CB}, its effect on I_B is negligible. As a consequence, input characteristics for various values of V_{CE} will give almost identical curves as shown in Fig. 14.23.

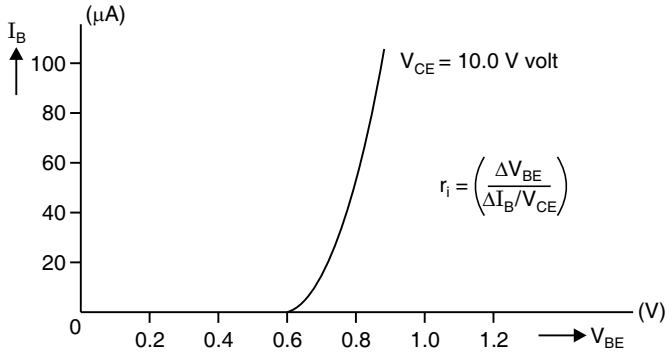


Fig. 14.23

(*ii*) Output characteristic is the study of variation of output current (I_C) with respect to output voltage (V_{CE}) keeping input current I_B constant. If V_{BE} is increased by a small amount, both hole current from the emitter region and the electron current from the base region will increase. As a consequence both I_B and I_C will increase proportionately. This shows that when I_B increases I_C also increases. The variation of I_C with respect to V_{CE} is shown in Fig. 14.24.

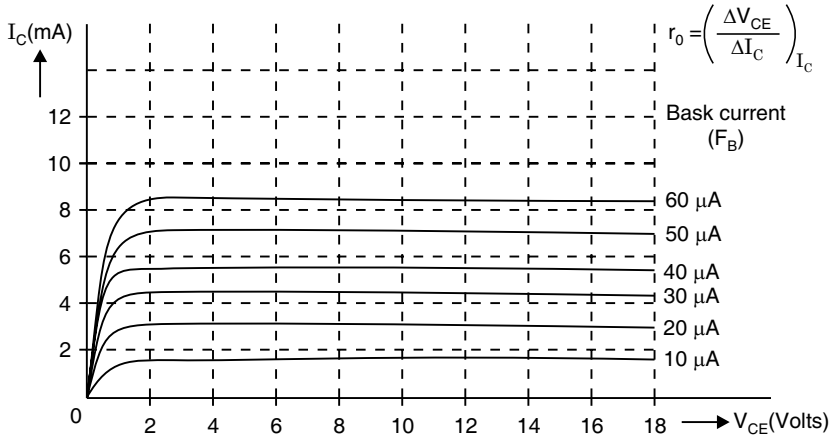


Fig. 14.24

(*iii*) **Transfer characteristics.** It is the study of change in output voltage with respect to change in input voltage. This variation is shown in Fig. 14.25.

In transfer characteristic there are three important regions:

(*a*) **Active region.** In the active region the collector-base junction is reversed biased while the base-emitter junction is forward biased.

(*b*) **Cut-off region.** In the cut-off region the collector base and base-emitter junctions of a transistor are both reverse biased.

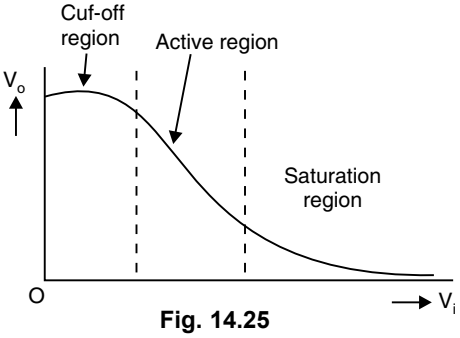


Fig. 14.25

(*c*) **Saturation region.** In saturation region the collector-base and base-emitter junctions are forward biased.

• Common Emitter Transistor as an Amplifier

To use transistor as an amplifier the circuit is made as shown in Fig. 14.26.

The signal which is to be amplified is applied across the input of the transistor and output is collected across collector and emitter.

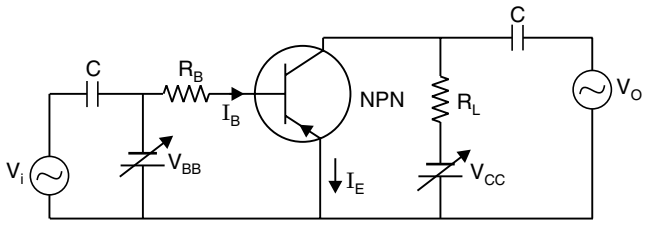


Fig. 14.26

For $V_i = 0$, applying the Kirchhoff's law to output loop,

$$V_{CC} = V_{CE} + I_C R_L \qquad ...(i)$$

and for input loop,

$$V_{BB} = V_{BE} + I_B R_B \qquad ...(ii)$$

When V_i is not zero,

$$V_{BB} = V_{BE} + V_i$$

So eqn. II becomes

$$V_{BE} + V_i = V_{BE} + I_B R_B + \Delta I_B (R_B + r_i)$$

The change in V_{BE} can be related to the input resistance r_i and the change in I_B.

$$\therefore \quad V_i = DI_B(R_B + r_i)$$
$$= r\Delta I_B$$

The change in I_B causes a change in I_C. If β is the ratio of change in output current to the change in input current called amplification factor, then

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{I_C}{I_B} \qquad ...(iii)$$

It is also known as current gain. The change in I_C due to a change in I_B causes change in V_{CE} and the voltage drop across the resistor R_L because V_{CC} is fixed.

These changes can be given by Eq. (*iv*) as

$$\Delta V_{CC} = \Delta V_{CE} + R_L \Delta I_C = 0$$

or $$\Delta V_{CE} = - R_L \Delta I_C \qquad (\because \quad \Delta V_{CE} = 0)$$

The change in V_{CE} is the output voltage V_0 will be

$$V_0 = DV_{CE} = - RL \frac{\Delta I_C}{\Delta I_B} \times \Delta I_B = - \beta R_L I_B$$

The voltage gain of the amplitude is

$$Av = \frac{V_0}{V_i} = \frac{\Delta V_{CE}}{r\Delta I_B}$$

$$= - \beta \frac{R_L}{r} \qquad ...(v)$$

The negative sign represents that output voltage is opposite with phase with the input voltage.

• Transistor as an Oscillator

In an oscillator a.c. output is obtained without any external input signal. The output in an oscillator is self-sustained. To attain this, an amplifier is taken. A portion of the output power is returned back to the input in phase with the starting power (positive feedback) so called feed back amplifier as shown in Fig. 14.27.

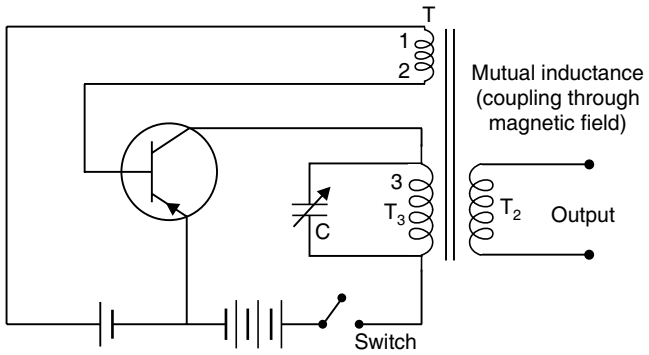


Fig. 14.27

The feedback can be achieved by inductive coupling through or *LC* or *RC* networks. Different types of oscillators essentially use different methods of coupling the output to the input, apart from the resonant circuit for obtaining oscillation at a particular frequency. In the circuit shown in Fig. 14.27 the feedback is accomplished by inductive coupling from one coil winding (T_1) to another coil winding (T_3). As in an amplifier, the base-emitter junction is reversed biased. In the circuit shown the tank or tuned circuit to produce the oscillations of desired frequency $\nu = \frac{1}{2\pi\sqrt{LC}}$ is connected in the collector side. Hence, it is also known as *tuned collector oscillator*. If the tuned circuit is on the base side, it will be known as *tuned base oscillator*. Due to resistance of transistor circuit the amplitude of oscillations sensed by tuned circuit keeps on decreasing and ultimately gets damped. To avoid this damping, the positive feed back is done through amplification action of the transistor to sustained the oscillations of desired frequency $\nu = \frac{1}{2\pi\sqrt{LC}}$.

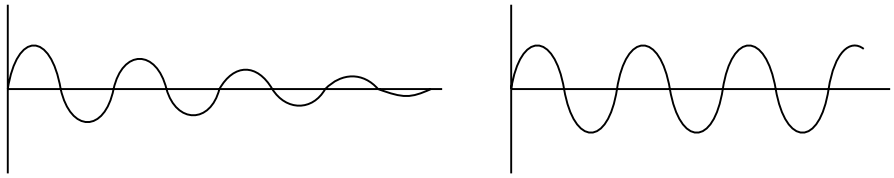


Fig. 14.28

• Transistor as a Switch

To use transistor as a switch the circuit is made as shown in Fig. 14.29.

Applying Kirchhoff's law to the input and output sides of the circuit.

$$V_{BB} = I_B R_B + V_{BE} \quad ...(i)$$

and $$V_{CC} = I_C R_C + V_{CE}$$

or $$V_{CE} = V_{CC} - I_C R_C \quad ...(ii)$$

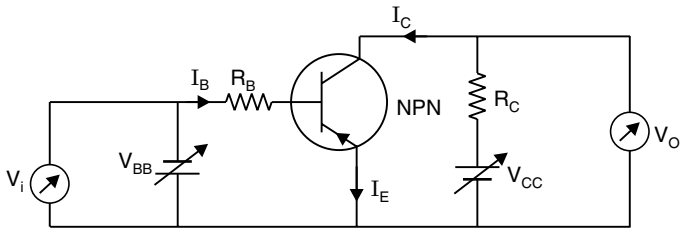


Fig. 14.29

V_{BB} can be considered as *dc* input voltage V_i and V_{CE} as *dc* output voltage V_0.

$\therefore \quad V_i = I_B R_B + V_{BB}$

and $\quad V_0 = V_{CC} - I_C R_L.$

In case of silicon transistor, as long as input V_i is less than 0.6 V, the transistor will be in cut-off state and current I_C will be zero.

$\therefore \quad V_0 = V_{CC}$

when V_i becomes greater than 0.6 V the transistor is in active region with some current I_C in the output path and the output V_0 decreases as the term $I_C R_C$ increases. With increase of V_i, I_C increases almost linearly and so V_0 decreases linearly till its value becomes less than about 1.0 V as shown in Fig. 14.30. Beyond this, the change becomes non-linear and transistor goes into saturation state. With further increase in V_i the output voltage is found to decrease farther towards zero though it may never becomes zero. Thus, the transistor in cut-off state acts as 'ON' and in saturated state as 'OFF'.

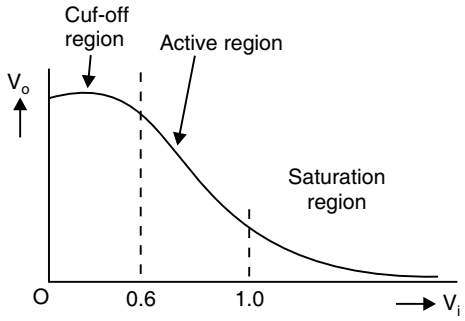


Fig. 14.30

• Logic Gates

It is a digital circuit that follows certain logical relationship between one or more than one input and the output.

These electronic devices work with the binary system of digits *i.e.*, '0' or low level and '1' or high level. They perform some logic operations.

Practically high level is attained by maintaining a wide difference between high level and low level. If the device is designed to operate at a maximum of 5V, then, the 'high level' is assigned at 4 ± 1V, while the 'low level' is at 0.2 ± 0.2 V. For some devices, the high level may be other than 4V.

'OR' Gate

The functional statement for 'OR' gate is the output (Y) of 'OR' gate will be 1 when the input A or B or both are 1.

The OR gate in terms of Boolean expression is

$$A + B = Y$$

(*i*) When $A = 0$, and $B = 0$, both diodes are reverse biased, hence $Y = 0$.

(*ii*) When $A = 0$, and $B = 1$, diode D_2 is forward biased, hence $Y = 1$.

(*iii*) When $A = 1$, and $B = 0$, diode D_1 is forward biased, hence $Y = 1$.

(*iv*) When $A = 1$, and $B = 1$, diode D_1 and D_2 are forward biased, hence $Y = 1$.

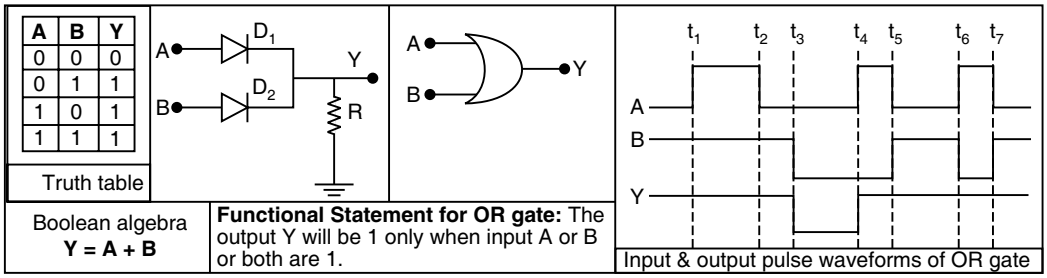


Fig. 14.31

'AND' Gate:

(*i*) When $A = 0$, and $B = 0$, both diodes are forward biased and conducts, hence voltage drops across R and $Y = 0$.

(*ii*) When $A = 0$, and $B = 1$, D_1 is forward biased and conducts, hence voltage drops across R and $Y = 0$.

(*iii*) When $A = 1$, and $B = 0$, D_2 is forward biased and conducts, hence voltage drops across R and $Y = 0$.

(*iv*) When $A = 1$, and $B = 1$, diode D_1 and D_2 are reverse biased, hence $Y = 1$.

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Truth table

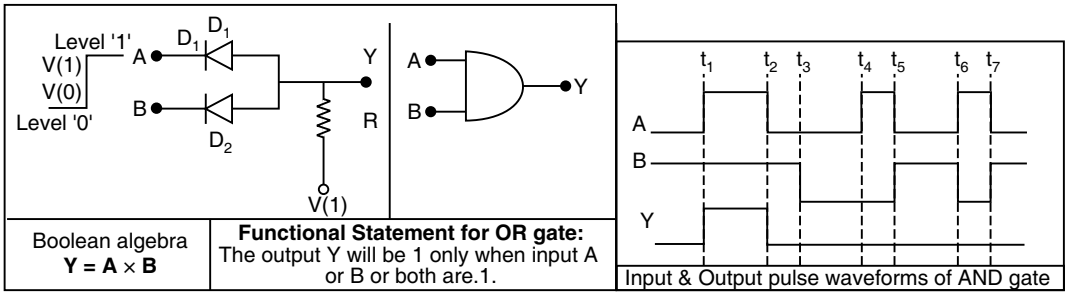


Fig. 14.32

'NOT' Gate

(*i*) When $A = 0$, the potential between R_1 and R_2 will be between '0' and '–1', hence the base will be more negative than the emitter and base-emitter will be reverse biased, hence the transistor will not conduct and voltage at $Y = 1$.

(*ii*) When $A = 1$, and R_1 and R_2 are so chosen that the potential between R_1 and R_2 is positive, then the base will be more positive w.r.t. the emitter and base-emitter will be forward biased, hence the transistor will conduct and voltage at $Y = 0$.

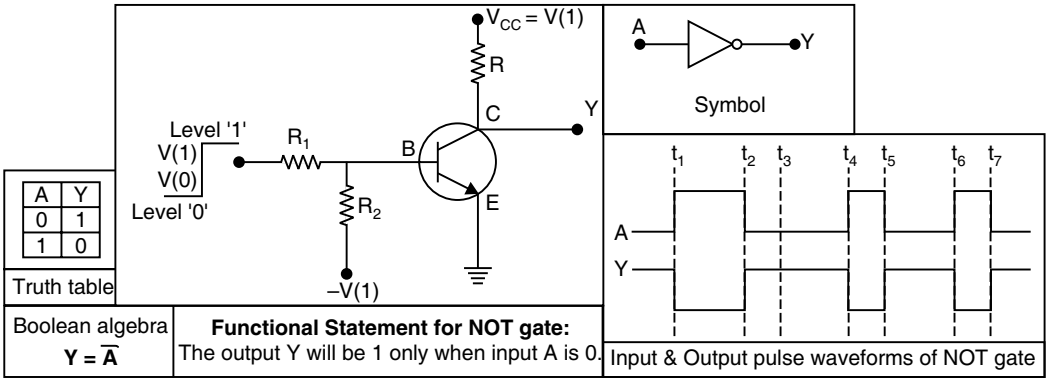


Fig. 14.33

'NOR' Gate

It is the combination of an 'OR' and a 'NOT' gate.

It is called universal gate as all the gates can be obtained from the combination of NOR gates.

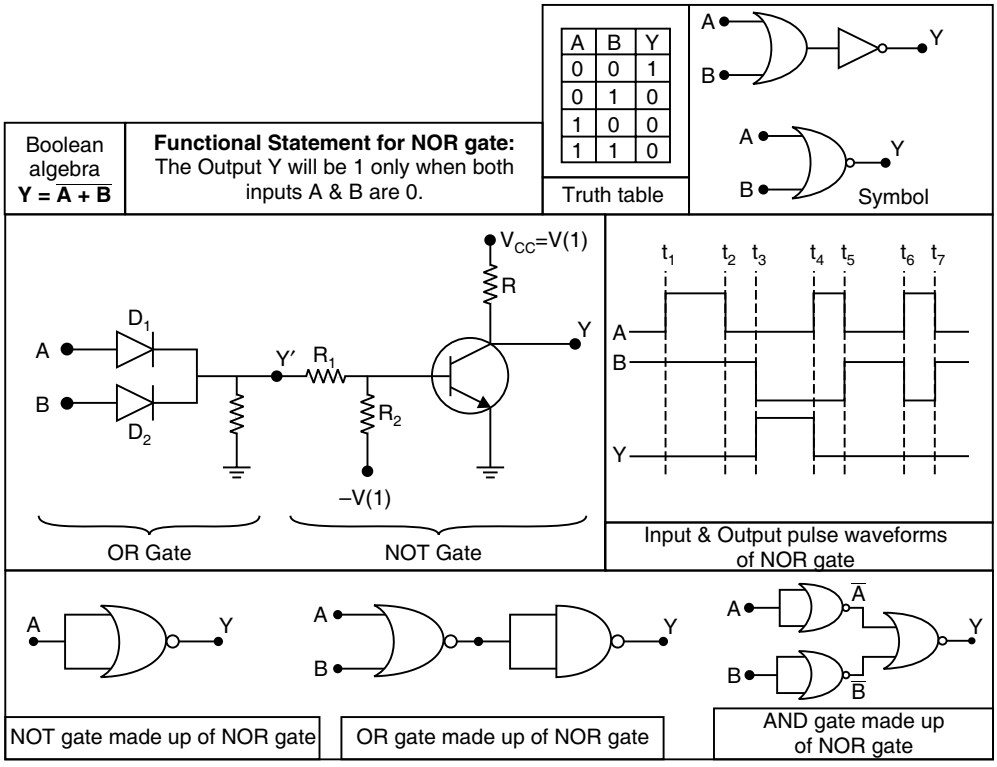


Fig. 14.34

'NAND' Gate

It is the combination of an 'AND' and a 'NOT' gate.

It is called universal gate as all the gates can be obtained from the combination of NAND gates.

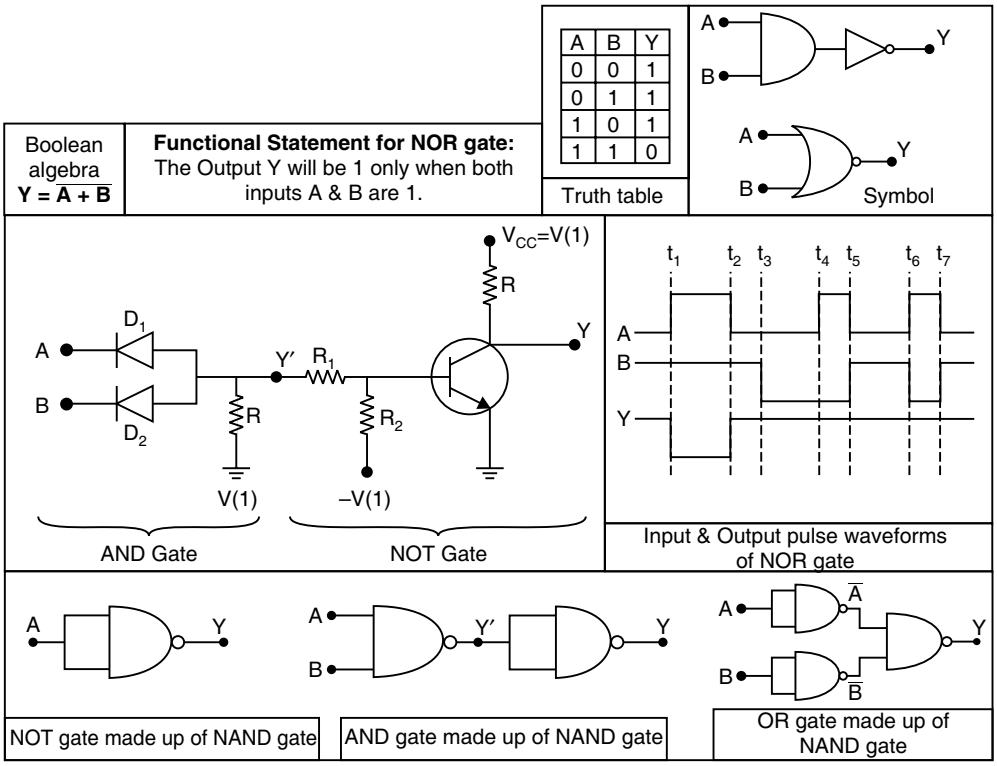


Fig. 14.35

QUESTIONS FROM TEXTBOOK

14.1. *In an n-type silicon, which of the following statement is true:*

(a) Electrons are majority carriers and trivalent atoms are the dopants.

(b) Electrons are minority carriers and pentavalent atoms are the dopants.

(c) Holes are minority carriers and pentavalent atoms are the dopants.

(d) Holes are majority carriers and trivalent atoms are the dopants.

Sol. *n*-type is obtained by doping the *Ge* or *Si* with pentavalent atoms. In *n*-type semiconductor, electrons are majority carriers and holes are minority carriers, hence answer (*c*) is true.

14.2. *Which of the statements given in Question 14.1 is true for p-type semiconductors.*

Sol. *p*-type semiconductor is obtained by doping *Ge* or *Si* with trivalent atoms. In *p*-type semiconductor holes are majority carriers and electrons are minority carriers. Hence (*d*) is correct.

14.3. *Carbon, silicon and germanium have four valence electrons each. These are characterised by valence and conduction bands separated by energy band gap respectively equal to* $(E_g)_C$, $(E_g)_{Si}$ *and* $(E_g)_{Ge}$. *Which of the following statements is true?*

(a) $(E_g)_{Si} < (E_g)_{Ge} < (E_g)_C$ *(b)* $(E_g)_C < (E_g)_{Ge} > (E_g)_{Si}$

(c) $(E_g)_C > (E_g)_{Si} > (E_g)_{Ge}$ *(d)* $(E_g)_C = (E_g)_{Si} = (E_g)_{Ge}$

Sol. (*c*) is correct.

As the energy band gap is maximum for carbon, less for silicon and least for germanium out of the given three elements.

14.4. *In an unbiased p-n junction, holes diffuse from the p-region to n-region because*

(a) free electrons in the n-region attract them.

(b) they move across the junction by the potential difference.

(c) hole concentration in p-region is more as compared to n-region.

(d) all the above.

Sol. (*c*) is correct.

As in an unbiased *p-n* junction, hole concentration in *p*-region is more than in *n*-region and due to difference in concentration they diffuse from *p*-region to *n*-region.

14.5. *When a forward bias is applied to a p-n junction, it*

(a) raises the potential barrier.

(b) reduces the majority carrier current to zero.

(c) lowers the potential barrier.

(d) none of the above.

Sol. When a forward bias is applied across the *p-n* junction, the applied voltage opposes the barrier voltage. Due to it, the potential barrier across the junction is lowered. Hence answer (*c*) is correct.

14.6. *For transistor action, which of the following statements are correct:*

(a) Base, emitter and collector regions should have similar size and doping concentrations.

(b) The base region must be very thin and lightly doped.

(c) The emitter junction is forward biased and collector junction is reverse biased.

(d) Both the emitter junction as well as the collector junction are forward biased.

Sol. Statements (*b*) and (*c*) are true.

For a transistor, $\beta = \dfrac{I_C}{I_B} \Rightarrow I_B = \dfrac{I_C}{\beta}$

$$R_i = \frac{V_i}{I_B} = \frac{V_i}{I_C}\beta, \quad i.e., \quad R_i \propto \frac{1}{I_c}.$$

Therefore, R_i depends upon collector current I_C. For a transistor action, the emitted junction is forward biased and collector junction is reverse biased.

14.7. *For a transistor amplifier, the voltage gain*

(a) remains constant for all frequencies.

(b) is high at high and low frequencies and constant in the middle frequency range.

(c) is low at high and low frequencies and constant at mid frequencies.

(d) None of the above.

Sol. (*c*) is correct.

For a transistor amplifier, the voltage gain is low at high and low frequencies and constant at mid frequencies.

14.8. *In half-wave rectification, what is the output frequency if the input frequency is 50 Hz. What is the output frequency of a full-wave rectifier for the same input frequency.*

Sol. Input frequency for half-wave and full-wave rectifier = 50 Hz.

Input and output waveforms of half-wave and full-wave rectifier are shown in figures (*a*) and (*b*).

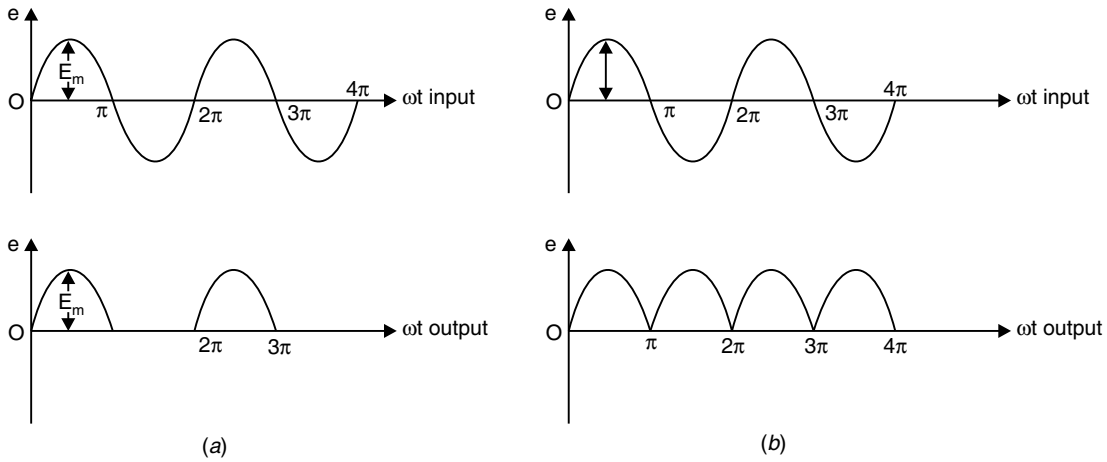


Fig. 14.36

Half-wave rectifier conducts once during a cycle and full-wave rectifier does so twice. Therefore, if input frequency is 50 Hz, output frequency for half-wave and full-wave rectifier are 50 and 100 Hz respectively.

14.9. *For a common emitter-transistor, amplifier, the audio signal voltage across the collector resistance of 2 kΩ is 2 V. Suppose the current amplification factor of the transistor is 100, find the input signal voltage and base current, if the base resistance is 1 kΩ.*

Sol. Here, $R_0 = 2000\ \Omega$; $V_0 = 2$ V, $\beta_{ac} = 100$; $V_i = ?$ $I_b = ?$ $R_i = 1000\ \Omega$

As, $$\boxed{A_v = \frac{V_0}{V_i}} = \beta_{ac}\frac{R_0}{R_i}$$

or, $$V_i = \frac{V_0}{\beta_{ac}\cdot(R_0/R_i)} = \frac{2}{100\,(2000/1000)} = 0.01\ \text{V}$$

$$\boxed{I_b = \frac{V_i}{R_i}} = \frac{0.01\,V}{1000\,\Omega} = 10\ \mu\text{A}$$

14.10. *Two amplifiers are connected one after the other in series (cascaded). The first amplifier has a voltage gain of 10 and the second has a voltage gain of 20. If the input signal is 0.01 V, calculate the output a.c. signal.*

Sol. Total voltage gain $A_V = \frac{\Delta V_0}{\Delta V_i} = A_{V_1} \times A_{V_2}$

or, $\Delta V_0 = \Delta V_i \times A_{V_1} \times A_{V_2} = 0.01 \times 10 \times 20 = 2$ V.

14.11. *A p-n photodiode is fabricated from a semiconductor with band gap of 2.8 eV. Can it detect a wavelength of 600 nm?*

Sol. Energy, $$\boxed{E = \frac{hc}{\lambda}} = \frac{6.6\times10^{-34}\times3\times10^{8}}{600\times10^{-9}\times1.6\times10^{-19}}\ \text{eV} = 2.06\ \text{eV} < 2.8\ \text{eV}$$

As $E < E_g$, so *p-n* junction cannot detect the radiation of given wavelength.

14.12. *The number of silicon atoms per m^3 is 5×10^{28}. This is doped simultaneously with 5×10^{22} atoms per m^3 of Arsenic and 5×10^{20} per m^3 atoms of Indium. Calculate the number of electrons and holes. Given that $n_i = 1.5 \times 10^{16}\ m^{-3}$. Is the material n-type or p-type?*

Sol. $n_e = 5 \times 10^{22} - 5 \times 10^{20} = (5 - 0.05) \times 10^{22}$

$$\boxed{n_h = \frac{n_i^2}{n_e}} = \frac{\left(1.5 \times 10^{16}\right)^2}{4.95 \times 10^{22}} = 4.54 \times 10^9 \text{ m}^{-3}$$

As $n_e > n_h$, so the material is *n*-type semiconductor.

14.13. *In an intrinsic semiconductor the energy gap E_g is 1.2 eV. Its hole mobility is much smaller than electron mobility and independent of temperature. What is the ratio between conductivity at 600 K and 300 K? Assume that the temperature dependence of intrinsic carrier concentration n_i is given* $\boxed{\text{by} \quad n_i = n_0 \exp\left(-\frac{E_g}{2k_BT}\right)}$, *where n_0 is a constant and $k_B = 8.62 \times 10^{-5}$ eV/K.*

Sol.
$$\frac{n_{i_1}}{n_{i_2}} = \frac{e^{\frac{1.2\,eV}{2 \times k_B \times 600}}}{e^{\frac{1.2\,eV}{2 \times k_B \times 300}}}$$

$$= e^{\frac{1.2\,eV}{2 \times k_B}\left(\frac{1}{300} - \frac{1}{600}\right)}$$

$$= e^{\frac{1.2 \times 1.6 \times 10^{-19}}{2 \times 1.381 \times 10^{-23} \times 600}}$$

or, $$\frac{n_{i_1}}{n_{i_2}} = e^{11.59} = 1.072 \times 10^5$$

(Let $x = e^{11.59} \Rightarrow \log x = 11.59 \log_e$

$\Rightarrow \log_{10} x = \frac{11.59}{2.303} = 5.03$

$x = \text{antilog } 5.03 = 1.072 \times 10^5$).

14.14. *In a p-n junction diode, the current I can be expressed as*

$$\boxed{I = I_0 \exp\left(\frac{eV}{2k_BT} - 1\right)}$$

where I_0 is called the reverse saturation current, V is the voltage across the diode and is positive for forward bias and negative for reverse bias, and I is the current through the diode, k_B is the Boltzmann constant (8.6×10^{-5} eV/K) and T is the absolute temperature. If for a given diode $I_0 = 5 \times 10^{-12}$ A and T = 300 K, then

(a) What will be the forward current at a forward voltage of 0.6 V?

(b) What will be the increase in the current if the voltage across the diode is increased to 0.7 V ?

(c) What is the dynamic resistance?

(d) What will be the current if reverse bias voltage changes from 1 V to 2 V?

Sol. Here, $I_0 = 5 \times 10^{-12}$ A, $T = 300$ K

$k_B = 8.6 \times 10^{-5}$ eVk^{-1} $= 8.6 \times 10^{-5} \times 1.6 \times 10^{-19}$ JK^{-1}

(*a*) If $V = 0.6$ V, then $\frac{eV}{k_BT} = \frac{1.6 \times 10^{-19} \times 0.6}{8.6 \times 10^{-5} \times 1.6 \times 10^{-19} \times 300} = 23.26$

$$I = I_0\left[\exp\left(\frac{eV}{k_BT}-1\right)\right] = 5 \times 10^{-12}\ [e^{23.26} - 1]$$

$$= 5 \times 10^{-12}\ [1.259 \times 10^{10} - 1]$$

$$= 5 \times 10^{-12} \times 1.259 \times 10^{10} = 0.063\ \text{A}$$

(*b*) If $V = 0.7$ V, then $\dfrac{eV}{k_BT} = \dfrac{1.6\times10^{-19}\times0.7}{8.6\times10^{-5}\times1.6\times10^{-19}\times300} = 27.14$

$$I = I_0\left[\exp\left(\frac{eV}{k_BT}-1\right)\right] = 5 \times 10^{-12}\ [e^{27.14} - 1]$$

$$= 5 \times 10^{-12}\ [6.07 \times 10^{11} - 1] = 5 \times 10^{-12} \times 6.07 \times 10^{11}$$

$$= 3.035\ \text{A}$$

$\therefore$ Increase in current, $\Delta I = (3.035 - 0.063) = 2.972$ A

(*c*) As, $\Delta I = 2.972$ A, $\Delta V = 0.7 - 0.6 = 0.1$ V

$$\text{Dynamic resistance} = \frac{\Delta V}{\Delta I} = \frac{0.1\ \text{V}}{2.972\ \text{A}} = 0.0336\ \Omega$$

(*d*) For both the voltages, the current I will be almost equal to I_0, showing almost infinite dynamic resistance in the reverse bias.

14.15. *You are given the two circuits as shown in figure. Show that circuit (a) acts as OR gate while the circuit (b) acts as AND gate.*

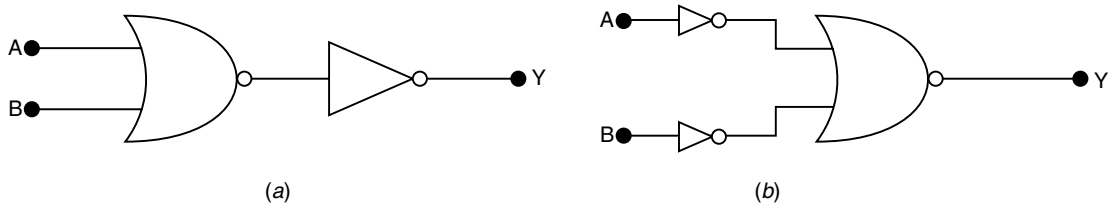


Fig. 14.37

Sol. (*a*) Here in figure (*a*) input A and B is given to NOR gate. So the output of NOR gate is Y'.

A	B	Y'
0	0	1
0	1	0
1	0	0
1	1	0

Now Y' is input for NOT gate. So output Y is represented in form of truth table as shown.

Input Y'	*Output* $Y = Y'$
1	0
0	1
0	1
0	1

Which is same as truth table of OR gate.

(*b*) Here in figure (*b*), input *A* and *B* are given to two NOT gates and these inverted input is provided to NOR gate.

Its truth table can be represented as

		Output of NOT gates	
A	***B***	$\overline{A}$	$\overline{B}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	0

Now output of NOT gate is fed as input to NOR gate. So its truth table can be represented as

Input		*Output*
$\overline{A}$	$\overline{B}$	Y
1	1	0
1	0	0
0	1	0
0	0	1

which represents AND operation.

14.16. *Write the truth table for a NAND gate connected as given in figure.*

Hence identify the exact logic operation carried out by this circuit.

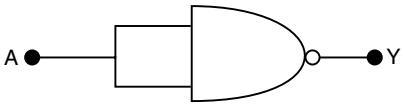


Fig. 14.38

Sol. The truth table for the circuit:

A	***Y***
0	1
1	0

This can be represented as $Y = \overline{A}$

The circuit represents the NOT gate.

14.17. *You are given two circuits as shown in figure, which consist of NAND gates. Identify the logic operation carried out by the two circuits.*

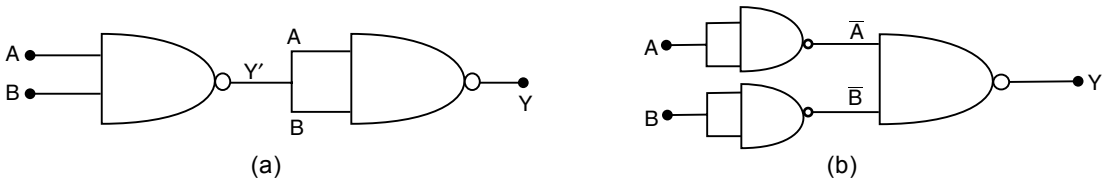


Fig. 14.39

Sol. The truth table for first circuit: (*a*)

A	*B*	*Y′*	*Y*
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

If we remove the intermediate output *Y′*, the overall result stands for the AND gate.

A	*B*	*Y*
0	0	0
0	1	0
10	0	0
1	1	1

Hence, the circuit is an equivalent of AND gate.

The truth table for second circuit: (*b*)

A	*B*	$\overline{A}$	$\overline{B}$	*Y*
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

If we remove the intermediate output $\overline{A}$ and $\overline{B}$, the overall result stands for the OR gate.

A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	1

This can be represented as $Y = A + B$

Hence, the circuit is an equivalent of OR gate.

14.18. *Write the truth table for circuit given in figure below consisting of NOR gates and identify the logic operation (OR, AND, NOT), which this circuit is performing.*

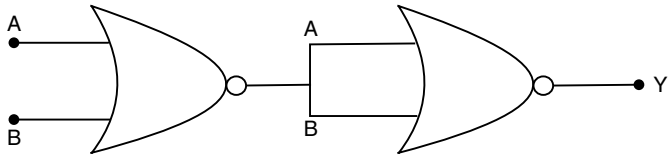


Fig. 14.40

*(***Hint:** *A = 0, B = 1 then A and B inputs of second NOR gate will be 0 and hence Y = 1. Similarly work out the values of Y for other combinations of A and B. Compare with the truth table of OR, AND, NOT gates and find the correct one.)*

Sol. In the given figure first portion represents NOR gate, second represents NOT gate. First we calculate output of 1 which acts as input for 2. 2 inverts it and we get final output Y.

A	B	$A + B$	$\overline{A + B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

A	B	$\overline{A + B}$	$Y = \overline{\overline{A + B}}$
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Which is truth table for OR gate.

14.19. *Write the truth table for the circuits given in figure. Consisting of NOR gates only. Identify the logic operations (OR, AND, NOT) performed by the two circuits.*

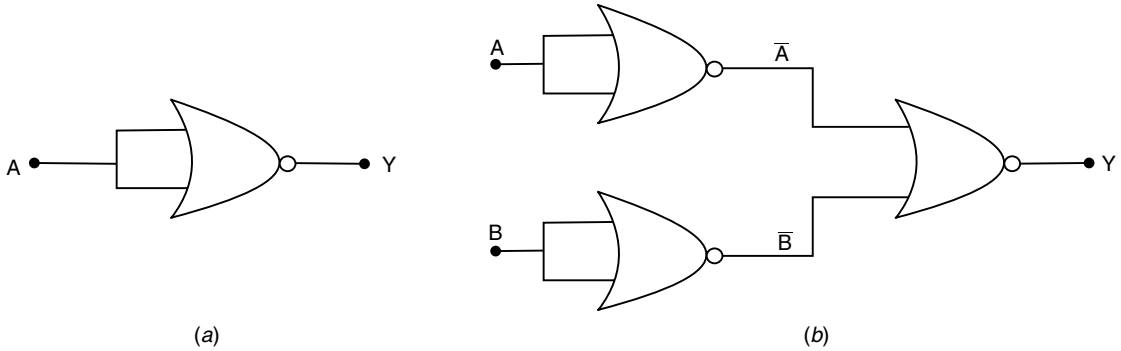


Fig. 14.41

Sol. Figure (*a*) represents NOT gate.

Here when $A = 1, \quad Y = 0$

and when $A = 0, \quad Y = 1$

Figure (*b*) represents two NOT gates whose outputs are given to NOR gate.

Its truth table is

A	B	$\overline{A}$	$\overline{B}$	Y
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

Y is truth table of AND gate.

Logic operation performed by figure (*b*) is AND operation.

MORE QUESTIONS SOLVED

I. VERY SHORT ANSWER TYPE QUESTIONS

Q. 1. *Give the logic symbol of AND gate.*

Ans.

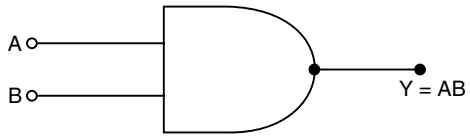


Fig. 14.42

This is the logic symbol of AND gate.

Q. 2. *Give the logic symbol of NAND gate.*

Ans.

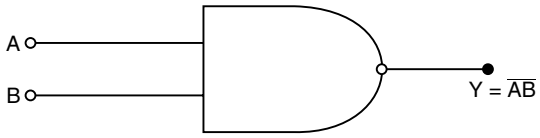


Fig. 14.43

Q. 3. *Why should a photodiode be operated at a reverse bias?*

Ans. In reverse bias condition of photodiode, the change in saturation reverse current is directly proportional to the change in the incident light flux, which can be measured accurately. When photodiode is in forward bias the condition is not the same.

Q. 4. *State the factor, which controls:*

(i) Wavelength of light and (ii) intensity of light emitted by an LED.

Ans. (*i*) Energy, hence the *wavelength of photons emitted depends upon the band gap.*

(*ii*) The forward current increases as the intensity of light increases and reaches a maximum. Further increase in the forward current results in decrease of light intensity. LEDs are biased such that the light emitting efficiency is maximum.

Q. 5. *At what temperature would an intrinsic semiconductor behave like a perfect insulator?*

Ans. At $T = OK$, an intrinsic semiconductor will behave like an insulator.

Q. 6. *Name the type of biasing of a p-n junction diode so that the junction offers very high resistance.*

Ans. Reverse biasing.

Q. 7. *A transistor has a current gain of 50. In a CE amplifier circuit, the collector resistance is chosen as 5 kilo ohms and the input resistance is 1 kilo ohm. Calculate the output voltage if input voltage is 0.01 V.*

Ans. Given,

Current gain, $\beta = 50; \quad R_C = 5\ \text{k}\Omega; \quad R_B = 1\ \text{k}\Omega;$

$v_i = 0.01\ \text{V}$

The voltage gain, $A_v = \dfrac{v_0}{v_i} = \beta \dfrac{R_C}{R_B}$

$\Rightarrow \quad v_0 = \beta \dfrac{R_C}{R_B} \times v_i = 50 \times \dfrac{5000}{1000} \times 0.01$

$= 2.5\ \text{V}.$

Q. 8. *Name one impurity each, which when added to pure Si, produces (i) n-type and (ii) p-type semiconductor.*

Ans. (*i*) As (Arsenic) (*ii*) In (Indium).

Q. 9. *Why is the conductivity of n-type semiconductor greater than that of the p-type semiconductor even when both of these have same level of doping?*

Ans. The conductivity of *n*-type semiconductor is greater than that of the *p*-type semiconductor because mobility of electrons is greater than that of holes.

Q. 10. *What is the main cause of electron's diffusion from n-type region to p-type region, even when there is no external supply used?*

Ans. Because of difference in free electron density and mobility between *n*-type and *p*-type region.

Q. 11. *Name two factors on which electrical conductivity of a pure semiconductor at a given temperature depends.*

Ans. Electrical conductivity of a pure semiconductor depends upon:

(*i*) The width of the forbidden band.

(*ii*) Intrinsic charge carrier concentration.

Q. 12. *How will collector current be affected on increasing the thickness of base in a transistor?*

Ans. The collector current will decrease.

Q. 13. *How does the d.c. current gain of a transistor change, if the width of the base region is increased?*

Ans. The *d.c.* current gain of a transistor decreases because rate of electron-hole recombination process in the base increases.

Q. 14. *The a.c. current gain of a transistor is 120. What is the change in the collector current in the transistor whose base current changes by 100 μA?*

Ans. $\beta_{ac} = \dfrac{\Delta I_C}{\Delta I_B}$

$\Rightarrow \quad \dfrac{\Delta I_C}{\Delta I_B} = 120 \quad \Rightarrow \quad \dfrac{\Delta I_C}{100\ \mu\text{A}} = 120$

or, $$\frac{\Delta I_C}{100 \times 10^{-6}} = 120$$

$$\therefore \quad \Delta I_C = 120 \times 100 \times 10^{-6} \text{ A} = 12 \times 10^{-3} \text{ A} = 12 \text{ mA}.$$

Q. 15. *In n-p-n transistor circuit the collector current is 10 mA. If 90% of the electrons emitted reach to the collector, find the base current and emitter current.*

Ans. $I_C = 10$ mA

$$I_C = 90\% \text{ of } I_E \Rightarrow I_C = \frac{90}{100} \times I_E$$

$$I_E = \frac{I_C \times 100}{90} = \frac{10 \text{ mA} \times 100}{90} = 11.11 \text{ mA}.$$

Q. 16. *What is the main cause of Zener breakdown?*

Ans. Internal field emission is the prime cause of Zener breakdown.

Q. 17. *What is the ratio of the number of holes and the number of conduction electrons in an intrinsic semiconductor?*

Ans. The ratio of the number of holes and the number of conduction electrons in an intrinsic semiconductor is one.

Q. 18. *What type of charge carriers are there in a p-type semiconductor?*

Ans. Holes are the majority charge carriers and free electrons are the minority charge carriers.

Q. 19. *What is doping?*

Ans. The deliberate addition of impurity to an intrinsic semiconductor is called doping.

Q. 20. *What type of charge carriers are there in a n-type semiconductor?*

Ans. Free electrons are majority charge carriers and holes are minority charge carriers in a *n*-type semiconductor.

Q. 21. *How many NAND gates are required to make one NOT gate?*

Ans. Only one NAND gate is required to make a NOT gate. If one input of a NAND gate is made permanently high, we get a NOT gate [see figure (*a*)].

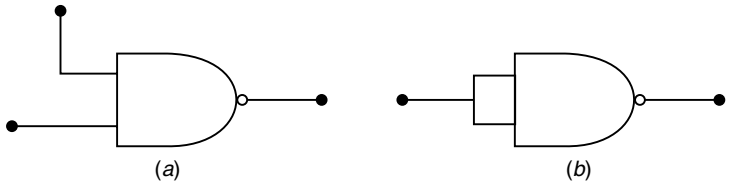


Fig. 14.44

Alternatively, if both the inputs of a NAND gate are tied together, we get a NOT gate. [see figure (*b*)].

Q. 22. *In a transistor, current gain for common base and common emitter configurations are α and β respectively. What is the relation between α and β?*

Ans. $\beta = \dfrac{\alpha}{1-\alpha}$.

Q. 23. *Using the concept of electron and hole current, write an expression for the conductivity of a semiconductor.*

Ans. $\sigma = n_e e\mu_e + n_h e\mu_h$.

Q. 24. *Why is NAND (or NOR) gate called a digital building block (or universal gates)?*

Ans. All types of gates can be prepared using NAND (or NOR) gates. Hence they are called digital building block (or universal gates).

II. SHORT ANSWER TYPE QUESTIONS

Q. 1. *(i) Sketch the output waveform from an AND gate for the inputs A and B shown in the figure.*

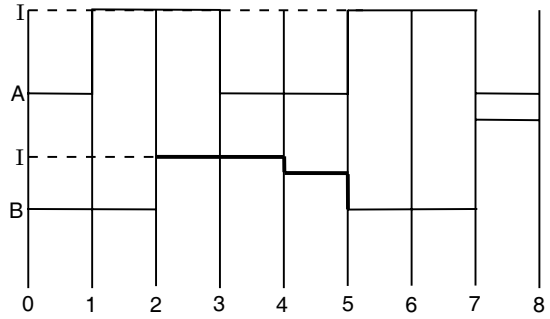


Fig. 14.45

(ii) If the output of the above AND gate is fed to a NOT gate, name the gate of the combination so formed.

Ans. (*i*) The output waveform of AND gate is given below.

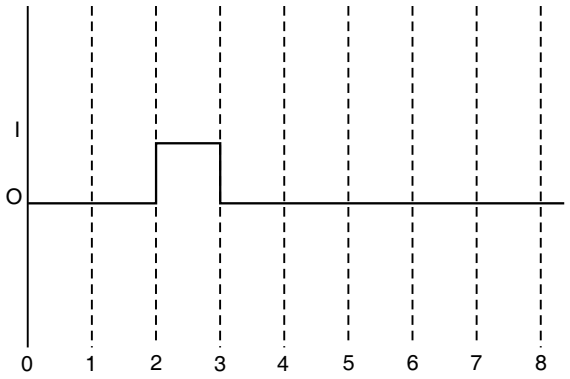
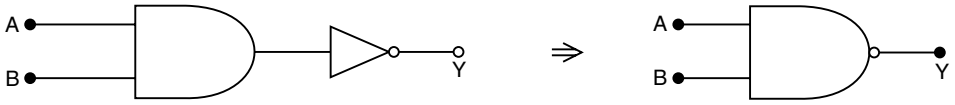


Fig. 14.46

(*ii*) The combination so formed will be NAND gate.

Q. 2. *The output of a 2 input AND gate is fed to a NOT gate. Give the name of the combination and its logic symbol. Write down its truth table.*

Ans. NAND gate is the combination.



Truth table:

A	B	$Y = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

Q. 3. *Draw the (i) symbol and (ii) the reverse I-V characteristics of a zener diode. Explain briefly, which property of the characteristics enables us to use Zener diode as voltage regulator.*

Ans. (*i*) Symbol of Zener diode:

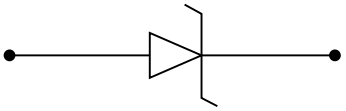


Fig. 14.50

(*ii*) *I-V* characteristics:

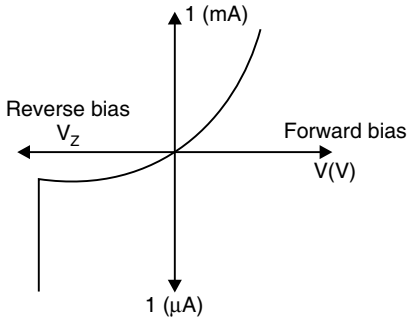


Fig. 14.47

Zener diode as voltage regulator:

For widely different Zener currents, the voltage across the Zener diode remains constant. On account of this fact we can use Zener diode as a *d.c.* voltage regulator.

For input voltage $V_i > V_z$, Zener diode is in the breakdown condition. Thus, for wide range of values of load (R_L), current through the Zener diode may change but the voltage across it remains constant.

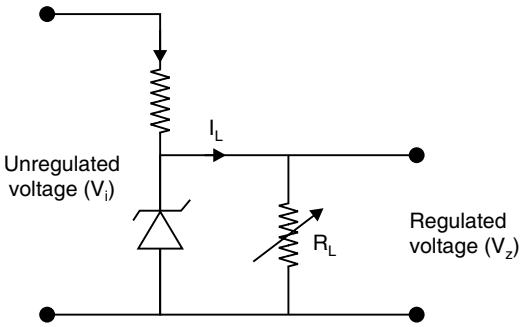


Fig. 14.48

Q. 4. *Draw the output wave form at X, using the given inputs A, B for the logic circuit shown below. Also identify the gate.*

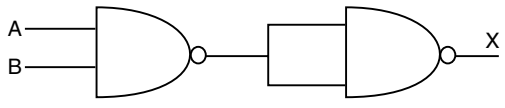


Fig. 14.49

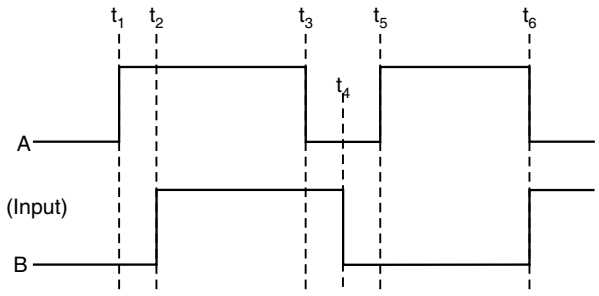


Fig. 14.50

Ans. NAND followed by a NOT represents an AND gate. Hence, the output waveform for the given input form will be:

AND gate

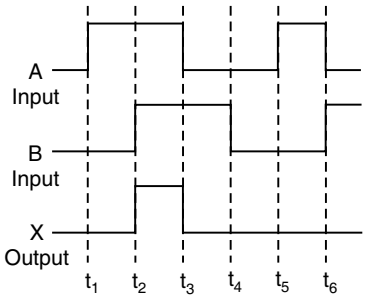


Fig. 14.51

Q. 5. *If the output of a 2 input NOR gate is fed as both inputs A and B to another NOR gate, write down a truth table to find the final output, for all the combinations of A, B.*

Ans. Output of NOR gate if fed to both inputs of another NOR gate.

A	*B*	*X*	*Y*
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

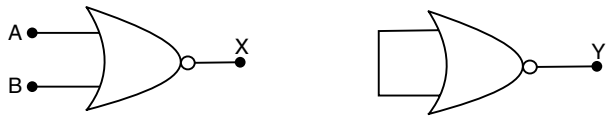
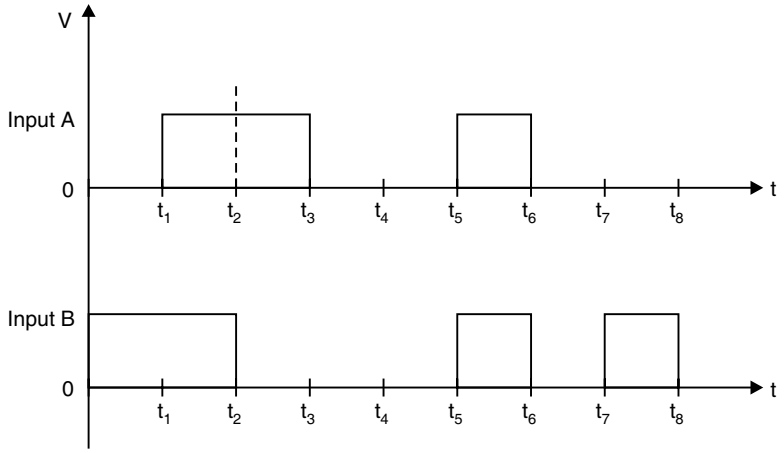


Fig. 14.52

Q. 6. *Two signals A, B as given below, are applied as input to (i) AND (ii) NOR and (iii) NAND gates. Draw the output waveform in each case.*



Ans.

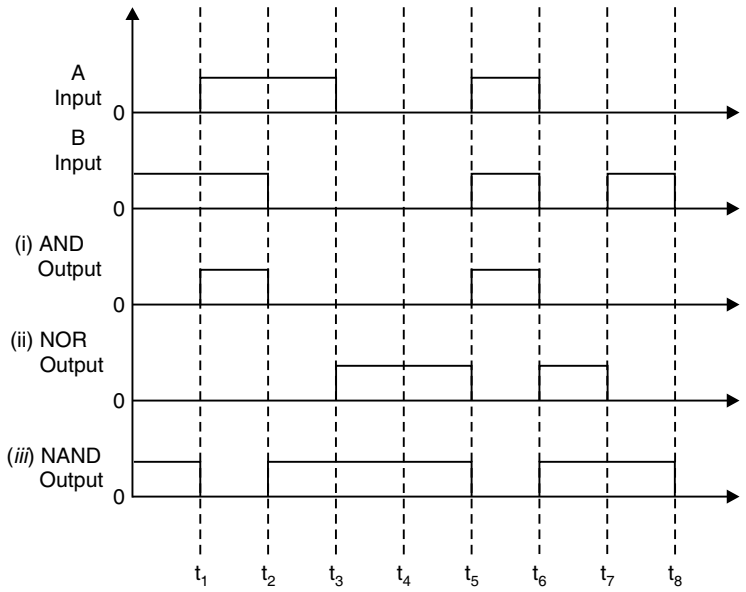


Fig. 14.53

Q. 7. *The output of an OR gate is connected to both the inputs of a NAND gate. Draw the logic circuit of this combination of gates and write its truth table.*

Ans. Logic circuit:

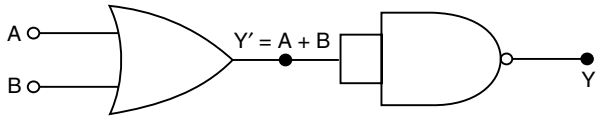


Fig. 14.54

Truth table:

A	B	$Y' = A + B$	$Y = \overline{Y'}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Q. 8. *Two semiconductor materials X and Y shown in the given figure, are made by doping germanium crystal with indium and arsenic respectively. The two are joined end to end and connected to a battery as shown.*

(i) Will the junction be forward biased or reverse biased?

(ii) Sketch a V - I graph for this arrangement.

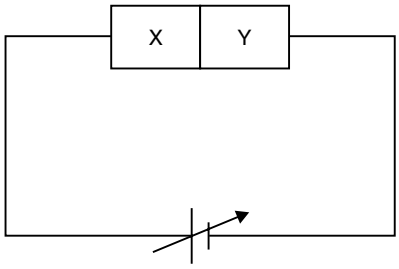


Fig. 14.55

Ans. (*i*) *X* is a *p*-type semiconductor and *Y* is an *n*-type semiconductor. So the junction is reverse biased.

(*ii*) The *V-I* graph for a reverse biased junction is given below:

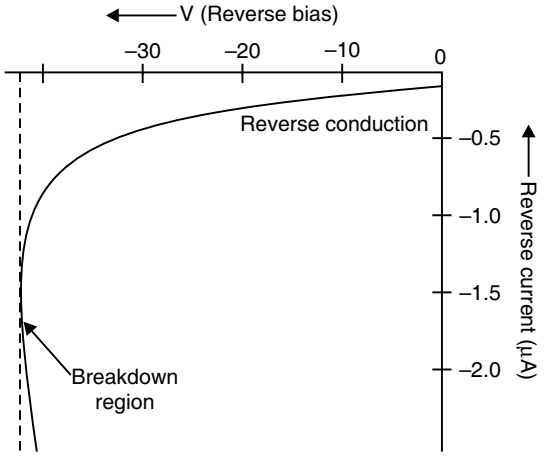


Fig. 14.56

Q. 9. *Draw and explain the output waveform across the load resistor R, if the input waveform is as shown in the given figure.*

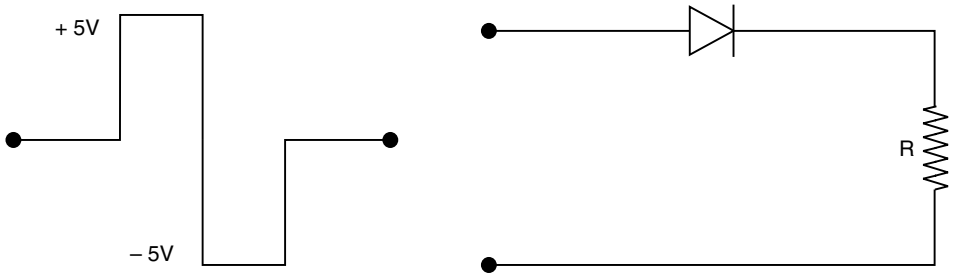


Fig. 14.57

Ans. When the input voltage is +5V, the diode gets forward biased, the output across R is +5V, as shown in figure. When the input voltage is –5V, the diode gets reverse biased. No output is obtained across *R*.

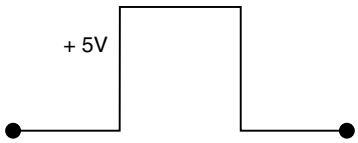


Fig. 14.58

Q. 10. *What is an intrinsic semiconductor? How can this material be converted into (i) P-type (ii) N-type extrinsic semiconductor? Explain with the help of energy band diagroms.*

Ans. See text.

Q. 11. *The output of an unregulated d.c. power supply is to be regulated. Name the device that can be used for this purpose and draw the relevant circuit diagram.*

Ans. Zener diode is used to regulate the output of an unregulated *d.c.* power supply. The relevant circuit diagram is given below.

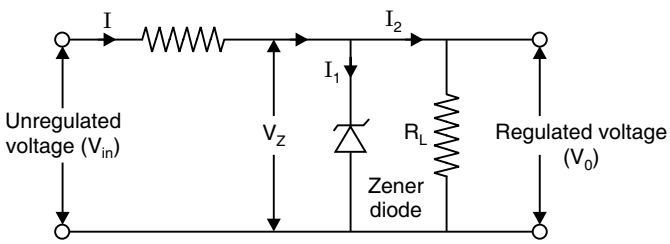


Fig. 14.59

Q. 12. *Identify the gate shown in the figure. Explain with the help of a circuit diagram, how this gate is realised in practice.*

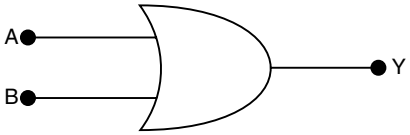


Fig. 14.60

Ans. OR gate

(*i*) When $A = 0$, and $B = 0$, both diodes are reverse biased, hence $Y = 0$.

(*ii*) When $A = 0$, and $B = 1$, diode D_2 is forward biased, hence $Y = 1$.

(*iii*) When $A = 1$, and $B = 0$, diode D_1 is forward biased, hence $Y = 1$.

(*iv*) When $A = 1$, and $B = 1$, diode D_1 and D_2 both are forward biased, hence $Y = 1$.

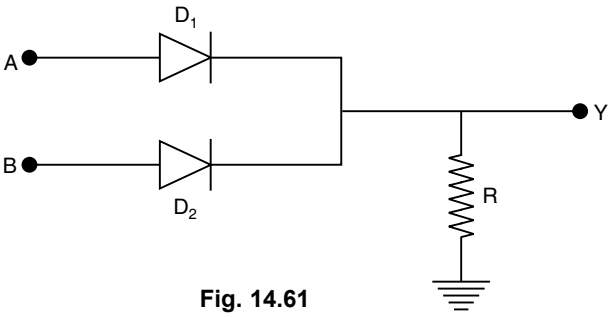


Fig. 14.61

Q. 13. *Explain, with the help of a circuit diagram, how the thickness of depletion layer in a p-n junction diode changes when it is forward biased. In the following circuits (fig. 14.62) which one of the two diodes is forward biased and which is reverse biased?*

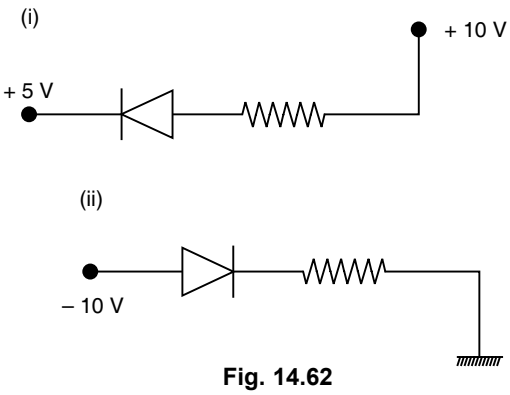
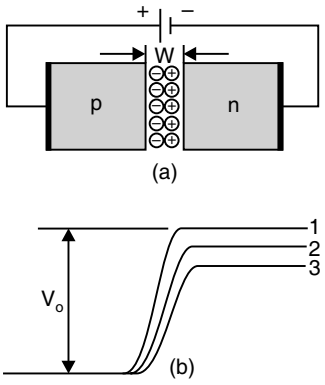


Fig. 14.62

Ans. When applied voltage is such that *n*-side is negative and *p*-side is positive, the applied voltage is opposite to the barrier potential. Hence, the effective barrier potential becomes V_B-V, and the energy barrier across the junction decreases. Thus, the junction width decreases.

(*i*) *p-n* junction is forward biased.

(*ii*) *p-n* junction is reverse biased.



(a) p-n junction diode under forward bias,
(b) Barrier potential
(1) without battery
(2) Low voltage battery, and
(3) High voltage battery,

Fig. 14.63

Q. 14. *Explain, with the help of a circuit diagram, how the thickness of depletion layer in a p-n junction diode changes when it is forward biased. In the following circuit which one of the two diodes is forward biased and which is reverse biased?*

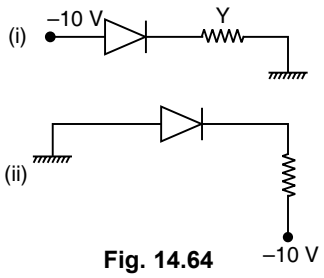


Fig. 14.64

Ans. Explanation is given in the previous answer.

(*i*) In this case, the *p*-side is at –10 V, whereas the *n*-side is at 0 V. $V_P < V_N$, hence, the diode is reverse biased.

(*ii*) In this case, the *p*-side is at 0 V, whereas the *n*-side is at –10 V. $V_P > V_N$, hence, the diode is forward biased.

Q. 15. *On the basis of the energy band diagrams distinguish between metals, insulators and semiconductors.*

Ans. See text.

Q. 16. *Justify the output wave form (Y) of the OR gate for inputs (A) and (B) as given in the following figure:*

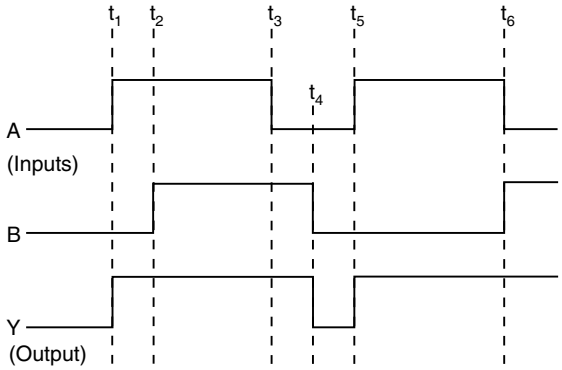


FIg. 14.65

Ans.

Time interval	Input A	Input B	Output, $Y = A + B$
$t < t_1$	0	0	0
$t_1 < t < t_2$	1	0	1
$t_2 < t < t_3$	1	1	1
$t_3 < t < t_4$	0	1	1
$t_4 < t < t_5$	0	0	0
$t_5 < t < t_6$	1	0	1
$t > t_6$	0	1	1

Q. 17. *Draw a circuit diagram for use of n-p-n transistor as an amplifier in common emitter configuration. The input resistance of a transistor is 1000 Ω. On changing its base current by 10 μA, the collector current increases by 2 mA. If a load resistance of 5 kΩ is used in the circuit, calculate:*

(i) the current gain,

(ii) voltage gain of the amplifier.

Ans. Circuit of *n-p-n* transistor as an amplifier in common emitter configuration is given below:

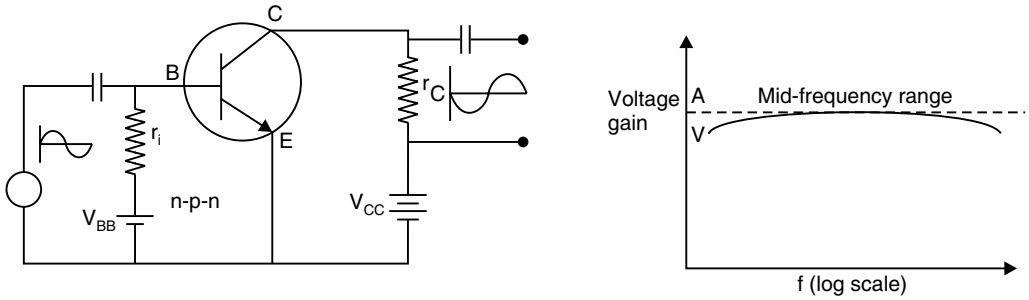


Fig. 14.66

Numerical:

Given, $\Delta I_B = 10\ \mu A;\quad \Delta I_C = 2\ mA;\quad R_L = 5\ k\Omega;\quad R_i = 1\ k\Omega;$

(*i*) The current gain, $\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}} = \frac{2\times10^{-3}}{10\times10^{-6}} = 200$

(*ii*) Voltage gain, $A_V = \beta\times\frac{R_L}{R_i} = 200\times\frac{5}{1} = 1000.$

Q. 18. *Mention two advantages and disadvantages of semiconductor devices.*

Ans. Advantages:

(*i*) Low cost (*ii*) No noise

Disadvantages:

(*i*) Cannot operate at high voltage (*ii*) Cannot operate at high current.

Q. 19. *Draw the energy band diagrams of p-type and n-type semiconductors.*
A semiconductor has equal electron and hole concentration $6\times10^8\ m^{-3}$. On doping with a certain impurity, electron concentration increases to $8\times10^{12}\ m^{-3}$. Identify the type of semiconductor after doping.

Ans.

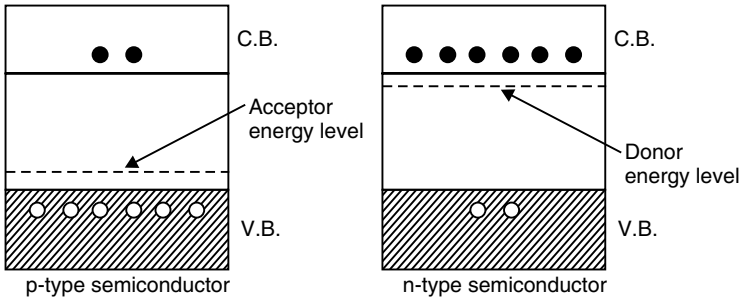


Fig. 14.67

As the electron concentration increases on doping, so the resulting semiconductor is of *n*-type.

Q. 20. *In a silicon transistor, a change of 7.89 mA in the emitter current produces a change of 7.8 mA in the collector current. What change in the base current is necessary to produce an equivalent change in the collector current?*

Ans. Given, $\Delta I_e = 7.89\ mA;\ \Delta I_c = 7.8\ mA$

Since, $\alpha_{ac} = \frac{\Delta I_c}{\Delta I_e} = \frac{7.8}{7.89} = 0.9886$

Now, $\beta_{ac} = \dfrac{\alpha}{1-\alpha} = \dfrac{0.9886}{1-0.9886} = 86.72$

Since, $\beta_{ac} = \dfrac{\Delta I_c}{\Delta I_b}$

$\Rightarrow \quad \Delta I_b = \dfrac{\Delta I_c}{\beta_{ac}} = \dfrac{7.8}{86.72} = 89.94 \times 10^{-3}$ mA.

Q. 21. *A change of 8.0 mA in the emitter current brings a change of 7.6 mA in the collector current. How much change in the base current is required to have the same change (= 7.6 mA) in collector current. Find the value of α and β.*

Ans. Given, $\Delta I_e = 8.0$ mA, $\Delta I_c = 7.6$ mA

As, $\Delta I_e = \Delta I_b + \Delta I_c$

or, $\Delta I_b = \Delta I_e - \Delta I_c$

$= 8.0 - 7.6 = 0.4$ mA

$$\alpha = \frac{\Delta I_c}{\Delta I_e} = \frac{7.6}{8.0} = 0.95$$

$$\beta = \frac{\Delta I_c}{\Delta I_b} = \frac{7.6}{0.4}$$

or, $\beta = 19.$

Q. 22. *For a common base amplifier, if the values of voltage gain and resistance gain are 2800 and 3000 respectively, find the current gain and power gain of this amplifier.*

Ans. Current gain $\alpha = \dfrac{\text{voltage gain}}{\text{resistance gain}}$

$\Rightarrow \quad \alpha = \dfrac{2800}{3000} = 0.93$

$$\text{Power gain} = \frac{(\text{voltage gain})^2}{\text{resistance gain}}$$

$$= \frac{(2800)^2}{3000} = 2613.3\,.$$

Q. 23. *In the following figure, circuit symbol of a logic gate and input waveform is shown in figure 14.68.*

(i) Name the logic gate, (ii) write its truth table and (iii) give the output waveform.

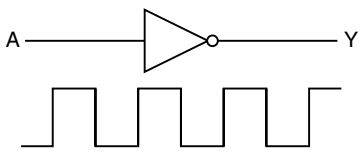


Fig. 14.68

Ans. (*i*) The logic gate is NOT gate.

(*ii*) Truth table of NOT gate

Input A	*Output* $\overline{Y} = \overline{A}$
0	1
1	0

(*iii*)

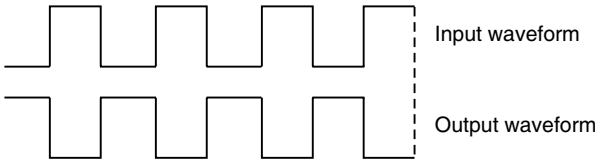


Fig. 14.69

Q. 24. *The gain of common-emitter amplifier is given by $A_V = -g_m R_L$. If R_L is increasing indefinitely, will the gain of the amplifier also increase indefinitely? Explain.*

Ans. No, if the load resistance is increased indefinitely, the output current will become zero. Hence, the voltage gain will be zero. (Here, g_m is called transconductance and is equal to current gain per unit input resistance.)

Q. 25. *In a transistor, connected in a common-emitter mode R_c = 4 kΩ; R_i = 1 kΩ; I_c = 1mA and I_b = 20 μA. Find the voltage gain.*

Ans. As, $\boxed{\beta = \frac{I_c}{I_b}} = \frac{10^{-3}}{20 \times 10^{-6}} = 50\,;$

voltage gain, $\boxed{A_V = \beta \frac{R_c}{R_i}} = 50 \times \frac{4000}{1000}$

$= 200.$

III. LONG ANSWER TYPE QUESTIONS

Q. 1. *(i) Draw a circuit diagram to study the input and output characteristics of an n-p-n transistor in its common emitter configuration. Draw the typical input and output characteristics.*

(ii) Explain, with the help of a circuit diagram, the working of n-p-n transistor as a common emitter amplifier.

Ans. (*i*) The variation of current on the input side with input voltage (I_B versus V_{BE}) is known as input characteristics, while the variation in the output current with output voltage ($I_c$versus V_{CE}) is known as output characteristics.

A simple circuit for drawing the input and output characteristics of an n-p-n transistor is shown in figure below. The corresponding input and output characteristics are also shown.

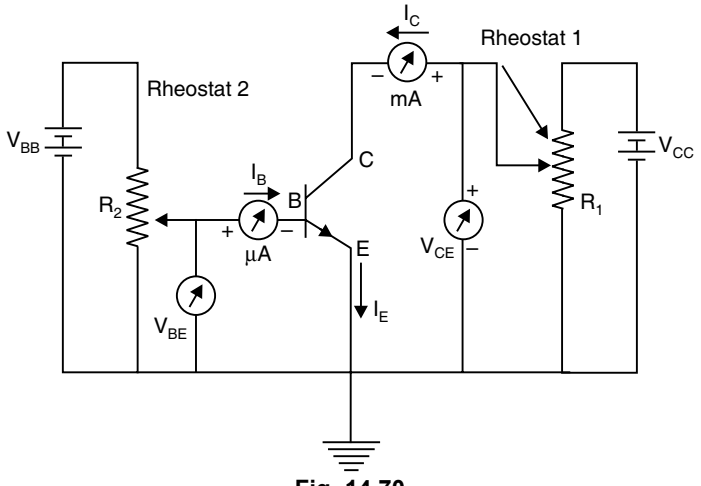


Fig. 14.70

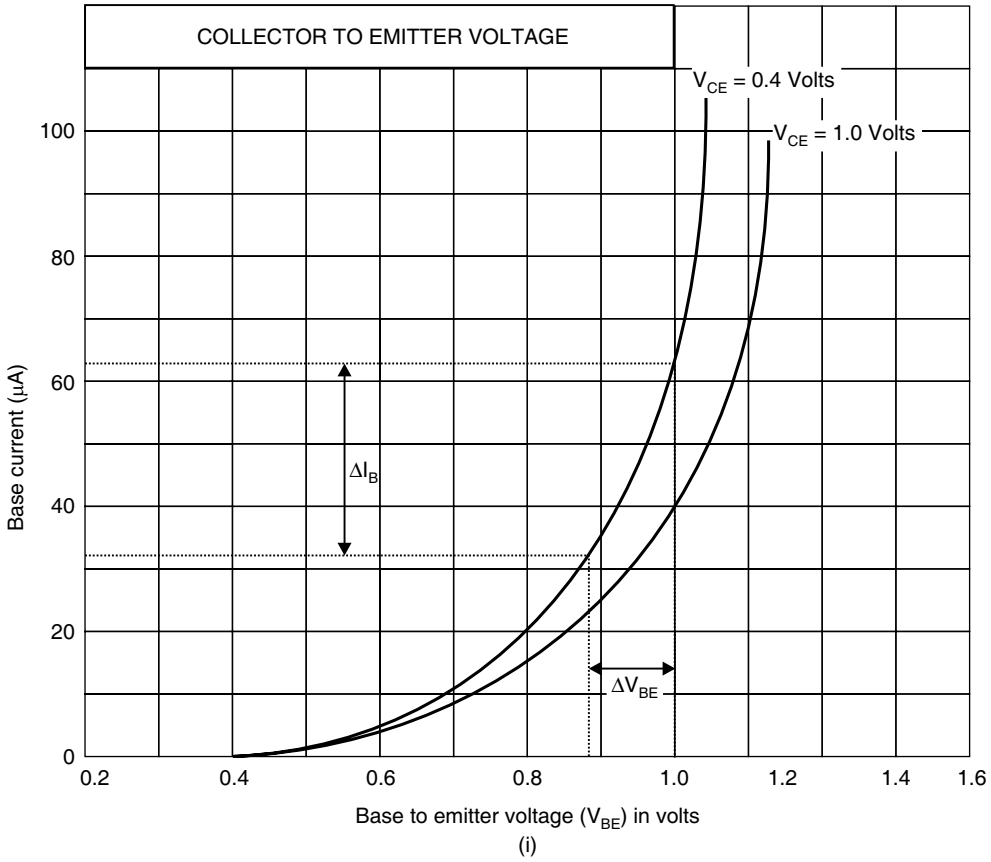


Fig. 14.71

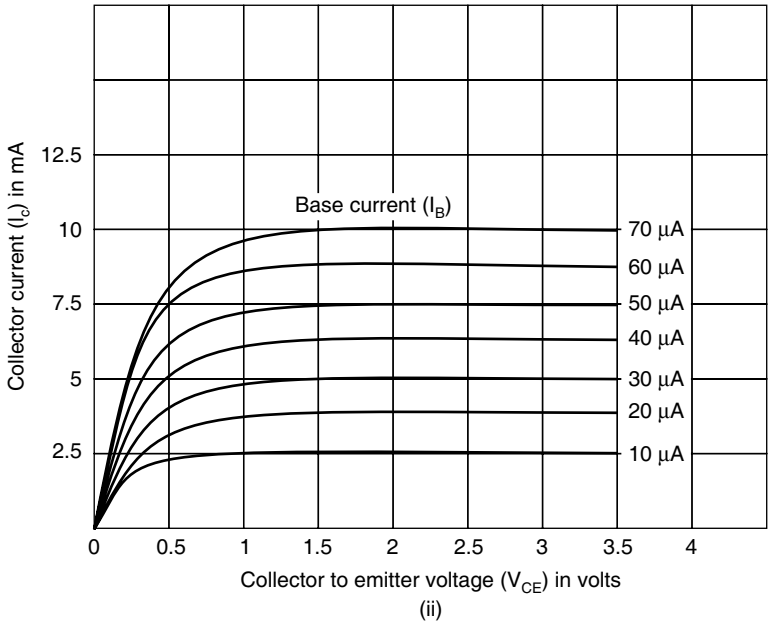


Fig. 14.72

(*ii*) Circuit diagram of a common emitter transistor amplifier is given below:

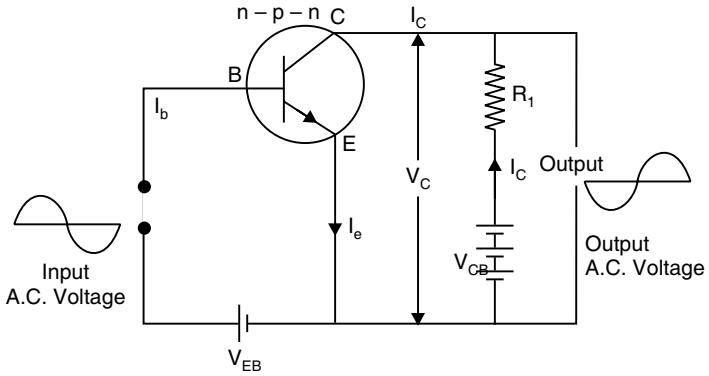


Fig. 14.73

The input (base emitter) circuit is forward biased and the output (collector emitter circuit is reverse biased.

When no a.c. signal is applied, the potential difference V_c between the collector and the emitter, is given by

$$V_c = V_{ce} - I_c \times R_L \qquad ...(i)$$

where V_{ce} is the voltage of battery V_{CE}.

when an a.c signal is fed to the input circuit, the forward bias increases during the positive half cycle of the input. This results in an increase in I_c and a consequent decreases in V_c, as is clear from equation (*i*).

Thus, during positive half cycle of the input, the collector becomes less positive.

During the negative half cycle of the input, the forward bias is decreased resulting in a decrease in I_E and hence I_C. Therefore, from (*i*) V_C would increase, making the collector more positive. Hence, in a common emitter amplifier, the output voltage is 180° out of phase with the input voltage.

Q. 2. *State the principle of working of p-n diode as a rectifier. Explain, with help of a circuit diagram, the use of p-n diode as a full wave rectifier. Draw a sketch of the input and output waveforms.*

Ans. The rectifier is a device that is capable of converting an alternating current into a unidirectional or pulsating form of direct current. The process of conversion of alternating currents into direct currents is known as rectification.

For principle of working and 'full wave rectifier', see text.

Q. 3. *Explain the function of base region of a transistor. Why is this region made thin and lightly doped? Draw a circuit diagram to study the input and output characteristics of n-p-n transistor in a common emitter (CE) configuration. Show these characteristics graphically. Explain how current amplification factor of the transistor is calculated using output characteristics.* (AI CBSE 2006)

Ans. The base provides proper interaction between the emitter and collector. The flow of majority charge carriers from emitter to the collector is controlled by the base of a transistor. Electron hole recombination takes place in the base region when emitter is forward biased. If the base is thin and lightly doped, it will have a small number density of majority charge carriers. This reduces the rate of electron hole recombination, necessary for a transistor action.

For a circuit diagram to study the input and output characteristics of *n-p-n* transistor in a *CE* configuration, see Answer Q.1 (Long Answer Type Questions).

Q. 4. *(a) Distinguish between metals, insulators and semiconductors on the basis of their energy bands.*
(b) Why are photodiodes used preferably in reverse bias condition? A photodiode is fabricated from a semiconductor with band gap of 2.8 eV. Can it detect a wavelength of 6000 nm? Justify.

Ans. (*a*) **Metals:** The energy band diagram for a metal is such that either the conduction band is partially filled with electrons, [see figure (*i*)] or the conduction and valence band partly overlap each other and there is no forbidden energy band gap in between.

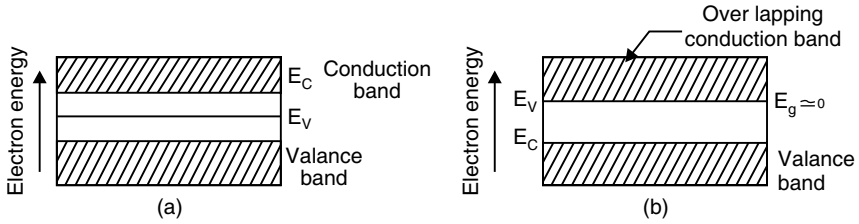


Fig. (*i*) Metals

Fig. 14.74

figure (*i*) *b*). In both the situations, it can be considered that the metal has a single energy band which is partly filled and partly empty.

Many electrons from below the Fermi level, by acquiring a little more energy from any source, can shift to the higher energy levels above the Fermi level in the conduction band and behave as free electrons. In this situation, large number of electrons are available for electrical conduction, hence the resistance of such a material is low or the conductivity is high. Even if a small electric field is applied across the metal, these free electrons start moving in a direction opposite to the direction of electric field. Due to it, a current begins to flow through it and hence metal behaves as a conductor.

Insulators: The energy bad diagram of insulator is shown in figure (*ii*). Here, the valence band is completely filled, the conduction band is empty and energy gap is quite large (E_g > 3 *eV*).

For example, in case of diamond, the energy gap is of 6 *eV*. Since, the valence band is completely filled as per Pauli's exclusion principle, therefore the electrons are not free. Again due to large energy gap, no electron is able to go from the valence band to the conduction band even if electric field is applied. Hence, electrical conduction in these materials is impossible and they behave as insulators.

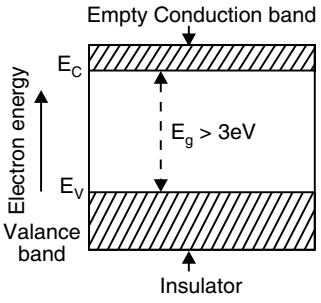


Fig. (*ii*)

Semiconductors: The energy band diagram of a semiconductor is shown in figure (*iii*). Here also, the valence band is totally filled and the conduction band is empty but the energy gap between conduction band and valence band is quite small. It is less than 3 *eV*. For example, the energy gap for germanium is of 0.72 eV and for silicon it is of 1.1 eV. At zero kelvin temperature, electrons are:

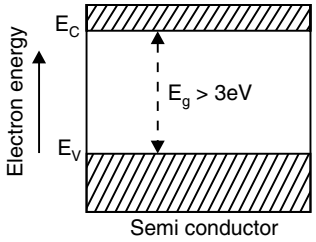


Fig. (*iii*)

Fig. 14.75

not able to cross even this small energy gap and hence the conduction band remains totally empty. Therefore, the

semiconductor at zero kelvin behaves as insulator. However, at room temperature, some electrons in the valence band acquire thermal energy greater than energy band gap less than 3 *eV* and jump over to the conduction band where they are free to move under the influence of even a small electric field. As a result of it, the semiconductor acquires small conductivity at room temperature. The resistance of semiconductor would not be as high as that of insulator.

(*b*) The fractional change due to the photoeffects on the minority carrier dominated reverse bias current is more easily measurable than the fractional change in the forward bias current. Hence, photodiodes are preferably used in the reverse bias condition for measuring light intensity.

Numerical:

$$\lambda = 6000 \text{ nm} = 6 \times 10^{-6} \text{ m}$$

Since, $$E = \frac{hc}{\lambda} = \frac{6.6 \times 10^{-34} \times 3 \times 10^{8}}{6 \times 10^{-6}} = 3.3 \times 10^{-20} \text{ J}$$

or, $$E = \frac{3.3 \times 10^{-20}}{1.6 \times 10^{-19}} = 0.206 \text{ eV}$$

As, the energy of the photon is less than E_g (= 2.8 eV) of the semiconductor, so a wavelength of 6000 A cannot be detected.

Q. 5. (*a*) *With the help of a circuit diagram explain the working of transistor as oscillator.*

(*b*) *Draw a circuit diagram for a two input OR gate and explain its working with the help of input, output waveforms.* (AI CBSE 2005)

Ans. (*a*) See Q. 3, Answer (Long Answer Type Questions).

(*b*) The OR gate can be made with the help of two *p-n* junction diodes D_1 and D_2 as given in the circuit follows.

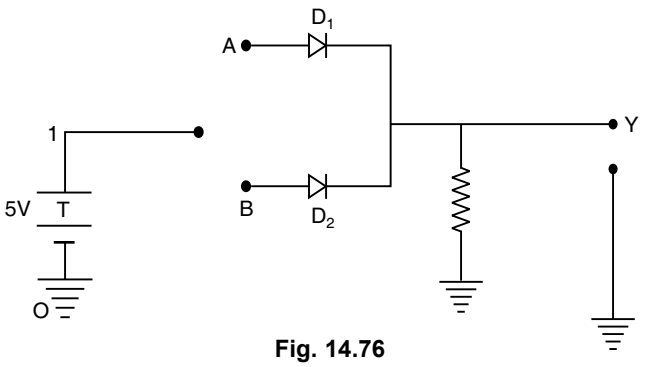


Fig. 14.76

Working: The negative terminal of the battery is gounded and corresponds to the 0 state and the positive (*i.e.*, voltage 5 V in the present case) to the 1 state.

When both *A* and *B* are connected to 0, no current passes through the diode and therefore no voltage develops across *R* and the output is zero.

When input *A* is connected to zero and *B* to 1, the diode D_2 is forward biased and the current through it is limited by a current limiting resistance. This current causes a 5 V drop across the resistance assuming the diode to be ideal and this gives an output of 5 V or 1. Interchanging *A* and *B* to 1 and 0 will still give a 5 V drop across the resistance as D_1 will conduct.

When the terminals *A* and *B* are connected to 1, then both the diodes D_1 and D_2 conduct. However, the voltage drop across *R* cannot exceed 5 V and the output is 1.

Q. 6. *For an n-p-n transistor in the common emitter configuration, draw a labelled circuit diagram of an arrangement for measuring the collector current as a function of collector emitter voltage for at least two different values of base current. Draw the shape of the curves obtained. Define the terms: (i) 'output resistance' and (ii) 'current amplification factor'*

Ans. Circuit diagram for drawing characteristics of a common emitter *n-p-n* transistor is given as follows:

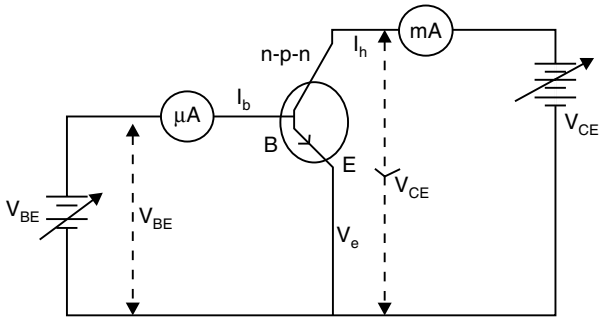


Fig. 14.77

The output characteristics are drawn by plotting current I_C versus collector emitter voltages V_{CE}, keeping the base current I_b constant in figure 14.78.

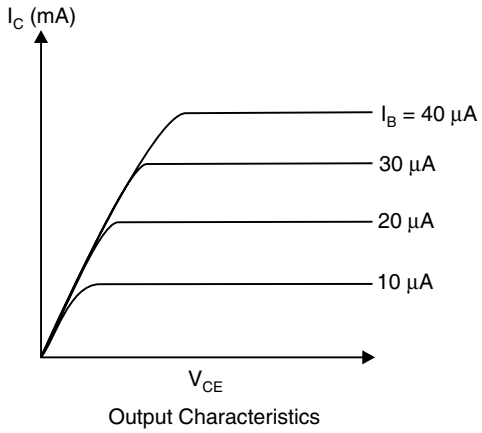


Fig. 14.78

Output resistance: It is defined as the ratio of the collector emitter voltage (ΔV_{CE}) to the corresponding change in collector current (ΔI_C) at constant base current I_b

$$R_0 = \left(\frac{\Delta V_{CE}}{\Delta I_c}\right)_{I_b = \text{constant}}$$

Current amplification factor: It is defined as the ratio of the change in collector current to the change in base current.

$$\beta = \left(\frac{\Delta I_{CE}}{\Delta I_b}\right)_{V_{CB} = \text{constant}}.$$

Q. 7. *Draw a circuit diagram of a common emitter amplifier using n-p-n transistor. Show the input and output voltage graphically.*

The current gain for common emitter amplifier is 59. If the emitter circuit is 6.0 mA, find (i) base current and (ii) collector current.

Ans. For circuit diagram, (See Q.1. long Answer Type Questions)

Numerical: Given, $\beta = 59$

Since, $\boxed{\alpha = \frac{\beta}{1+\beta}} = \frac{59}{60}$

But $\boxed{\alpha = \frac{I_C}{I_E}}$

$$\Rightarrow \qquad I_C = \alpha \cdot I_E$$

$$\text{or,} \qquad I_C = \frac{59}{60} \cdot 6\text{mA} = 5.9 \text{ mA}$$

$$I_B = I_E - I_C = 6.0 - 5.9 = 0.1 \text{ mA}.$$

Q. 8. *(a) Distinguish between intrinsic and extrinsic semiconductors.*

(b) Using a suitable combination from a NOR, an OR and a NOT gate. Draw circuits to obtain the truth table given below:

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	0

(*i*)

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	1

(*ii*)

Ans. (*a*) For distinction between intrinsic and extrinsic semiconductors, see text.

(*b*) (*i*) Circuit diagram for truth table (fig-14.79):

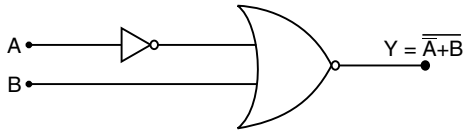


Fig. 14.79

Verification:

A	B	$\overline{A}$	$\overline{A}+B$	$Y=\overline{\overline{A}+B}$
0	0	1	1	0
0	1	1	1	0
1	0	0	0	1
1	1	0	1	0

(*ii*) Circuit diagram for truth table.

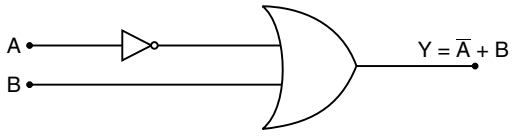


Fig. 14.80

Verfication:

A	B	$\overline{A}$	$Y=\overline{A}+B$
0	0	1	1
0	1	1	1
1	0	0	0
1	1	0	1

Q. 9. *(a) What is a p–n junction? How is a p–n junction made?*

(b) The given circuit diagram shows a transistor configuration along with its output characteristics. Identify

(i) the type of transistor used and

(ii) the transistor configuration employed.

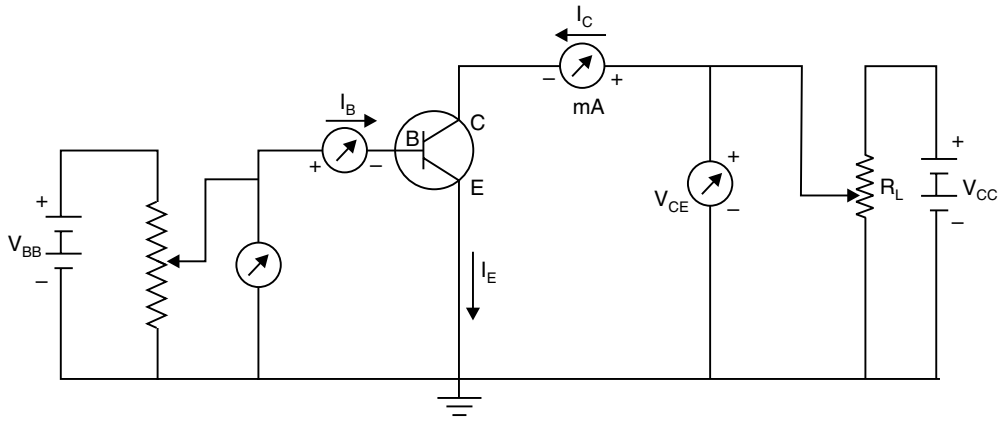


Fig. 14.81

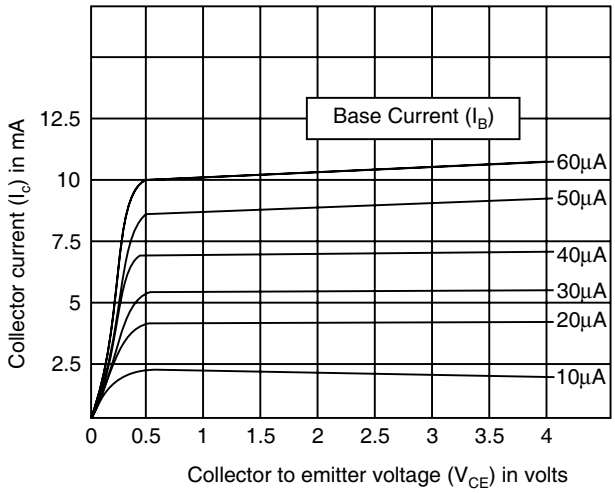


Fig. 14.82

Use these graphs to obtain the approximate value of current amplification factor for the transistor at V_{CE} = 3V.

Ans. (*a*) For p-n junction and its formation, see text.

(*b*) (*i*) *n-p-n* transistor is used.

(*ii*) Common emitter (*CE*) configuration.

Numerical: Current amplification factor is given by

$$\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{\text{at } V_{CE}}$$

$$\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{\text{at } V_{CE}\,=\,3V}$$

$$\Rightarrow \quad \beta_{ac} = \frac{(9.5-2.5)mA}{(60-10)\mu A}$$

$$= \frac{7.0\times10^{-3}}{50-10^{-6}} = 140.$$

QUESTIONS ON HIGH ORDER THINKING SKILLS (HOTS)

Q. 1. *The ratios of number density of free electron to holes,* $\left(\frac{n_e}{n_h}\right)$*, for two different materials A and B, are equal to one and less than one respectively. Name the type of semiconductors to which A and B belong. Draw energy level diagram for A and B.*

Ans. A is intrinsic semiconductor and *B* is p-type semiconductor.

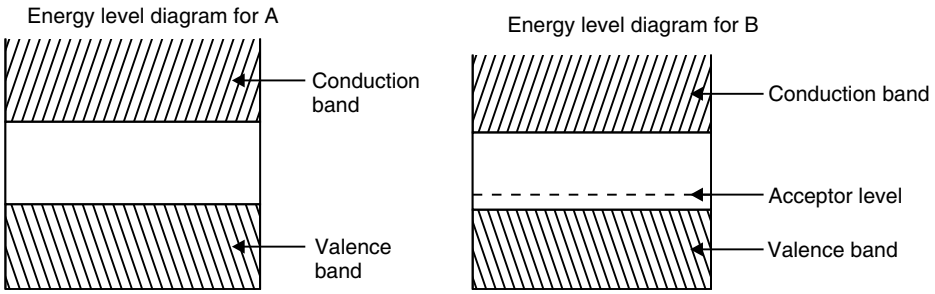


Fig. 14.83

Q. 2. *A Zener diode has a contact potential of 0.8 V in the absence of biasing. It undergoes Zener breakdown for an electric field of* 10^6 *Vm*$^{-1}$ *at the depletion region of p–n junction. If the width of the depletion region is 2.4 μm, what should be the reverse biased potential for the Zener breakdown to occur?*

Ans. Here, the breakdown electric field of the Zener diode,

$$E = 10^6 \text{Vm}^{-1}.$$

The width of the depletion region,

$$d = 2.4 \times 10^{-6} m$$

$$\therefore \quad V_{\text{Breakdown}} = E \times d$$

$$= 10^6 \times 2.4 \times 10^{-6} = 2.4 \text{ V}.$$

Q. 3. *From the output characteristics shown in figure calculate the values of current amplification factor of the transistor when* V_{CE} *is 2V.*

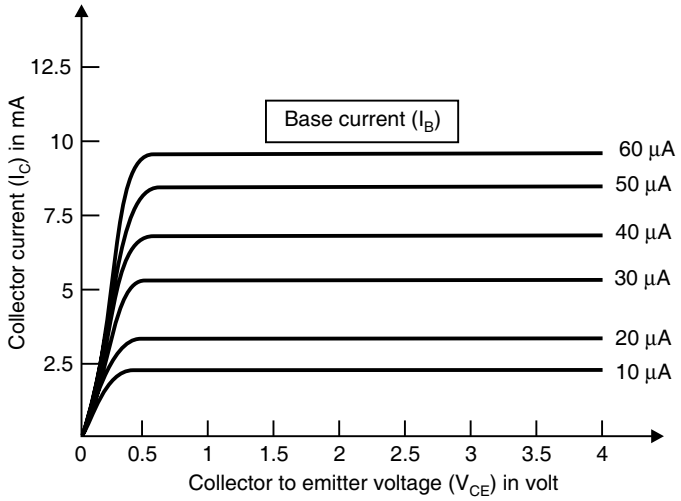


Fig. 14.84

Ans. As, $\boxed{\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}}$

Consider characteristics for any two values of I_B (say, 10 and 60 μA). Then for V_{CE} = 2 V from the graph, we have

$$\Delta I_B \approx (60 - 10)\ \mu A = 50\ \mu A$$
$$\Delta I_C \approx (9.5 - 2.5)\ mA = 7.0\ mA$$

Therefore, $$\beta = \left(\frac{7\times10^{-3}A}{50\times10^{-6}A}\right) = 140.$$

Q. 4. *Calculate the value of V_o and I if the Si diode and the Ge diode conduct at 0.7V and 0.3V respectively, in the circuit given in figure. If now Ge diode connections are reversed, what will be the new values of V_o and I.*

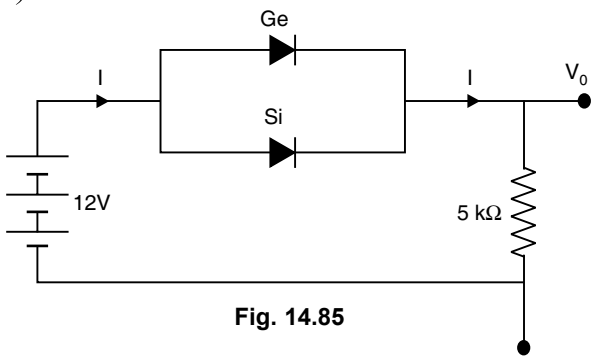


Fig. 14.85

Ans. Refer to the given circuit,

Current, $$I = \frac{12-0.3}{5\ k\ \Omega} = \frac{11.7V}{5\times10^3\Omega} = 2.34\ mA$$

Output voltage, $V_0 = RI = (5 \times 10^3) \times (2.34 \times 10^{-3}) = 11.7V$

When the connections of Ge diode are reversed, then current will be through silicon.

In this case, $$I = \frac{(12-0.7)V}{5\ k\ \Omega} = \frac{11.3V}{5\times10^3\Omega} = 2.26\ mA$$

$$V_0 = IR = (2.26 \times 10^{-3}) \times (5 \times 10^3) = 11.3V.$$

Q. 5. *An a.c. supply of 230 V is applied to a half-wave rectifier circuit through a transformer of turn ratio 10: 1. Find the output d.c. voltage. Assume the diode to be ideal.*

Ans. Here, $n_p/n_s = 10$; R.M.S. primary voltage, $V_{rms} = 230\ V$

Maximum primary voltage, $\boxed{V_{pm} = \sqrt{2} \times V_{rms}} = \sqrt{2} \times 230 = 325.3\ V$

Maximum secondary voltage, $\boxed{V_{sm} = V_{pm} \times \frac{n_s}{n_p}} = 325.3 \times \frac{1}{10} = 32.53\ V$

Half-wave rectified current,

$$\boxed{I_{d.c} = \frac{I_0}{\pi}}$$

$\therefore$ Output d.c. voltage $= I_{d.c.} \times R_L$

$$= \frac{I_0}{\pi} \times R_L = \frac{V_{sm}}{\pi}$$

$$= \frac{32.53}{3.14} = 10.36\ V.$$

Q. 6. *For a CE-transistor amplifier, the audio signal voltage across the collector resistance of 2 k Ω is 2V. If the current amplification factor of the transistor is 100, calculate (i) input signal voltage (ii) base current. Given that the value of the base resistance is 1 kΩ.*

Ans. (*i*) $\boxed{A_v = \beta \frac{R_C}{R_B}} \Rightarrow A_v = 100 \times \frac{2000}{1000} = 200$

$\boxed{V_0 = A_v \times V_i}$

$\Rightarrow \quad V_i = \frac{V_0}{A_v} = \frac{2}{200} = \frac{1}{100} V = 0.01 V$

(*ii*) Again, $\boxed{\beta = \frac{I_C}{I_B}}$

$\Rightarrow \quad I_B = \frac{I_C}{\beta} = \frac{V_0}{R_c} \times \frac{1}{\beta}$

$= \frac{2}{2000 \times 100} = \frac{1}{10^5} A = 10^{-5}\text{A}$

or, $I_B = 10 \times 10^{-6}\ A = 10\ \mu A.$

Q. 7. *Show that a bubbled OR gate is equivalent to a NAND gate. Hence prove the identity.*

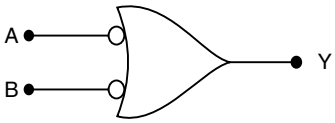


Fig. 14.86

Ans. A bubbled OR gate is the combination of two NOT gates and one OR gate *i.e.,* the output of two NOT gates is made as input of OR gate. The Boolean expression for output of this gate is $y = \overline{A} + \overline{B} = \overline{A \,.\, B}$ (From De-Morgan's Theorem). This expression is for NAND gate. Hence, a bubbled OR gate is equivalent to a NAND gate.

Q. 8. *State the basic electronic circuit involved in the electronic circuit of figure and find the value of the output y. Name the gate formed and set up a truth table for it.*

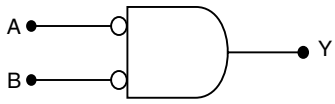


Fig. 14.87

Ans. The electronic circuit shown is a bubbled AND gate. It is a combination of two NOT gates and one AND gate, *i.e.,* the output of two NOT gates is made as input of AND gate. The Boolean expression for output of this gate is

$y = \overline{A} \,.\, \overline{B} = \overline{A + B}$ (From De-Morgan's Theorem).

This expression is for NOR gate. Hence, a bubbled AND gate is equivalent to a NOR gate. Truth table of this gate is as shown in the table.

A	B	$A + B$	$y = \overline{A+B}$
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

Q. 9. *In figure 14.88, a battery of emf 2V is used. The length of the block is 0.1m and the area is $1 \times 10^{-4} m^2$. If the block is of intrinsic silicon at 300 k, find the electron and hole currents.*

What will be the magnitude of the total current? What will be the magnitude of total current if germanium is used instead of silicon?

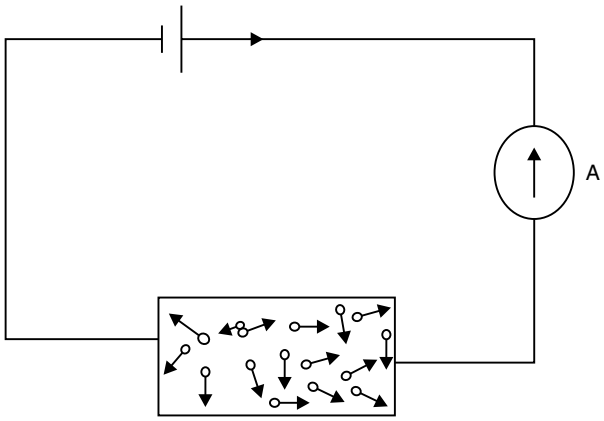


Fig. 14.88

Given–For silicon:

Mobility of electrons = 0.135 SI units

Mobility of holes = 0.048 SI units

Number density of electrons holes

$= 1.5 \times 10^{16}$ *per unit volume*

For germanium:

Mobility of electrons = 0.39 SI units

Mobility of holes = 0.19 SI units

Number density of electrons holes $= 2.4 \times 10^{19}$ *per unit volume*

Ans. We know the current i, due to charge carriers of density n and having charge e through a block of cross-section area A, is

$$\boxed{i = n\,A\,e\,v} \qquad ...(i)$$

where v is the average drift speed of the charge carriers.

The mobility μ of charge carriers is velocity acquired per unit external field E, *i.e,*

$$\boxed{\mu = \frac{v}{E}}$$

or, $$v = \mu E \qquad ...(ii)$$

The electric field E, is due to the applied potential V,

and $$\boxed{E = \frac{V}{l}} \qquad ...(iii)$$

From equations (*i*), (*ii*) and (*iii*), we have

$$i = n\,A\,e\mu \left(\frac{V}{l}\right)$$

For silicon, (for electrons)

$\mu_1 = 0.135$ *SI* units, $n = 1.5 \times 10^{16}$ per unit volume

For electron current i_1 is

$$i_1 = An_1 e\mu_1 \left(\frac{V}{l}\right)$$

$$= \frac{10^{-4} \times 1.5 \times 10^{16} \times 1.6 \times 10^{-19} \times 0.135 \times 2}{0.1}$$

$$= 6.45 \times 10^{-7}\ \text{A} = 0.645\ \mu A$$

Similarly, for holes μ_2 = 0.048 SI units and the hole current i_2 is

$$i_2 = \frac{10^{-4} \times 1.5 \times 10^{16} \times 1.6 \times 10^{-19} \times 0.048 \times 2}{0.1}$$

$$= 2.304 \times 10^{-7} = 0.2304 \ \mu A$$

The total current,

$$i = i_1 + i_2$$

$$= 0.645 + 0.2304 = 0.8754 \ \mu A$$

For germanium,

n = 2.4×10^{19} per unit volume,

μ_1' = mobility of electrons = 0.39 SI units

$\therefore$ i_1' = electronic current

$$= \frac{2.4 \times 10^{19} \times 10^{-4} \times 1.6 \times 10^{-19} \times 0.39 \times 2}{0.1}$$

$$= 2.99 \times 10^{-3} A = 2.99 \ mA$$

The mobility μ_2' of holes in germanium = 0.19 SI units

i'_2 = the hole current

$$= \frac{10^{-4} \times 2.4 \times 10^{19} \times 1.6 \times 10^{-19} \times 0.19 \times 2}{0.1}$$

$$= 1.49 \times 10^{-3} \text{ A} = 1.49 \ mA$$

$\therefore$ The total current i' is

$$i' = i_1' + i_2'$$

$$= 2.99 + 1.49 = 4.48 \ mA.$$

Q. 10. *Assume that the silicon diode in the given circuit (fig-14.89) requires a minimum current of 1 mA to be above the knee point (0.7 V) of its I–V characteristics. Also assume that the voltage across the diodes is independent of the current above the knee point.*

(a) If V_B = 5 V, what should be the maximum value of R so that the voltage is above the knee point?

(b) If V_B = 5 V, what should be the value of R to establish a current of 5mA in the circuit ?

(c) What is the power dissipated in the resistance R and in the diode, when a current of 5 mA flows in the circuit at V_B = 6 V.

(d) If R = 1 kΩ, what is the minimum voltage V_B required to keep the diode above the knee point?

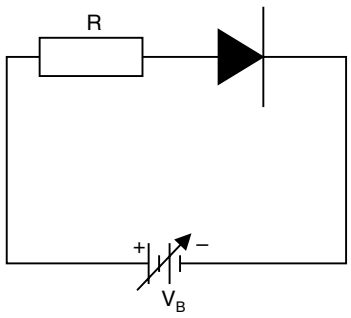


Fig. 14.89

Ans. (*a*) Since the minimum voltage across the diode is 0.7 *V* (so that it is above the knee point of the characteristic curve), the voltage drop across the resistance R = (5 – 0.7) V = 4.3 V. The minimum current i = 1 mA = 10^{-3} A.

$\therefore$ $$R = \frac{v}{i} = \frac{4.3}{10^{-3}} \Omega = 4.3 \ k\Omega.$$

(*b*) The current through the resistance R = 5 mA = 5×10^{-3} A

Also the voltage drop across R = (5 – 0.7) V = 4.3 V

$$R = \frac{4.3}{5\times10^{-3}}$$
$$= 0.86 \times 10^{-3}\ \Omega = 860\ \Omega$$

(*c*) Since V_B = 6 V, the voltage v' across the resistance is

$$v' = 6 - 0.7 = 5.3\ \text{V}$$

Current $i = 5\ \text{mA} = 5 \times 10^{-3}\ \text{A}$

The power, p, dissipated through the resistance R is

$$P = i\,v'$$
$$= 5 \times 10^{-3} \times 5.3\ \text{W}$$
$$= 26.5 \times 10^{-3}\ \text{W} = 26.5\ \text{mW}$$

The power, P'', dissipated in the diode is

$$P' = i \times 0.7\ \text{W} = 5 \times 10^{-3} \times 7 \times 10^{-1}\ \text{W}$$
$$= 3.5 \times 10^{-3}\ \text{W} = 3.5\ \text{mW}$$

(*d*) For keeping diode above the knee point, the minimum current required is 1 mA

$$V_R = \text{voltage drop across } R\ (= 1\ \text{k}\Omega)$$
$$= 1 \times 10^3 \times 10^3 = 1\ \text{V}$$

Also the minimum voltage drop across the diode = 0.7 V

$$\therefore \quad V_B = (1 + 0.7)\ \text{V} = 1.7\ \text{V}.$$

Q. 11. *The characteristic curve of a diode is shown in the above figure. Determine the d.c. and a.c. resistance around point.*

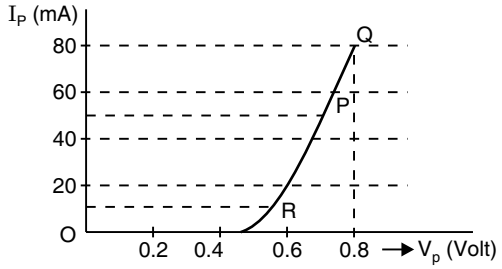


Fig. 14.90

Ans. d.c. resistance

$$r_{dc} = \frac{0.5}{5\times10^{-3}} = 100\ \Omega$$

a.c. resistance

$$r_{ac} = \frac{0.8 - 0.5}{(80 - 20)\times10^{-3}}$$
$$= \frac{0.3}{60\times10^{-3}} = 5\ \Omega$$

Q. 12. *The following figure shows the V–I characteristics of a semiconductor diode*

(i) Identify the semiconductor diode used.

(ii) Draw the circuit diagram to obtain the given characteristic of this device.

(iii) Briefly explain how this diode can be used as a voltage regulator.

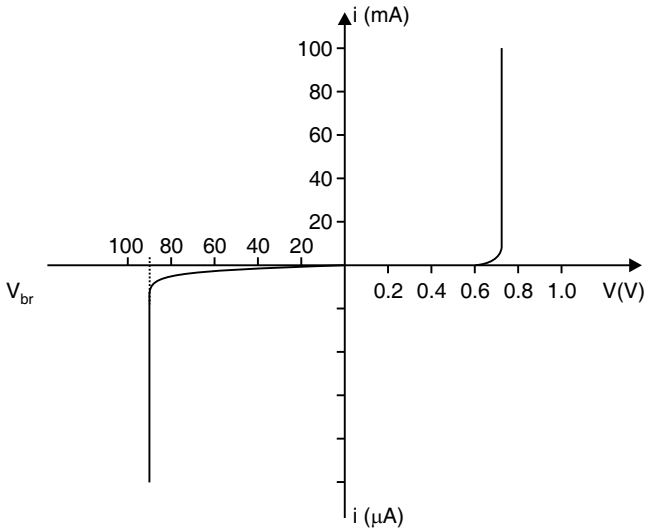


Fig. 14.91

Ans. (*i*) The semiconductor diode whose *V-I* characteristic is shown in the figure is Zener diode.

(*ii*) Circuit diagram to obtain the given characteristic is shown in Fig. 14.92.

(*iii*) The circuit of Zener diode used as voltage regulator is shown in Fig. 14.93.

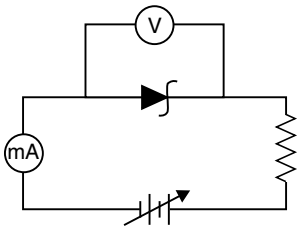


Fig. 14.92

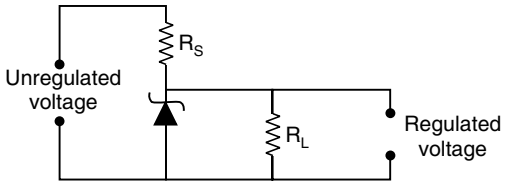


Fig. 14.93

The voltage to be regulated is applied across Zener diode as shown in circuit. When input voltage increases the current in Zener diode circuit increases and voltage drop across series resistance R_s increases and across R_L remain same *i.e.,* the voltage drop across Zener diode. Similarly when voltage decreases, the current in the Zener diode circuit decreases and voltage drop across series R_s resistance decreases but across the load resistance remains same, hence the voltage is regulated.

Q. 13. *Identify the gate equivalent to the 'dotted box' shown here and give its symbol and truth table.*

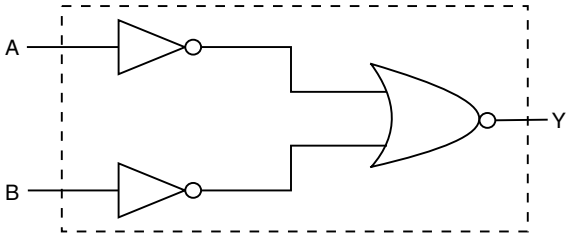


Fig 14.94

The inputs A and B shown here, are used as the two inputs in this set up. Give the shape of the output Y obtained from these inputs.

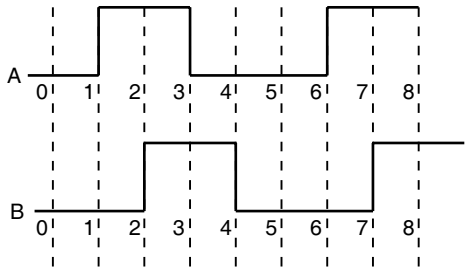


Fig. 14.95

Ans. The truth table of the gates combination is as below

A	B	$\overline{A}$	$\overline{B}$	$\overline{\overline{A}+\overline{B}}$
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

The given gates combination works as AND gate

The shape of output y is shown in figure 14.96.

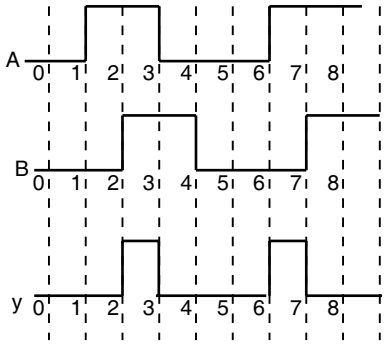


Fig. 14.96

Q. 14. *The black box, shown here, converts the input voltage waveform into the output voltage waveform as is shown in the figure 14.97.*

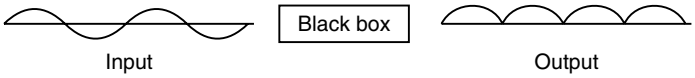


Fig. 14.97

Draw the circuit diagram of the circuit present in the black box and give a brief description of its working.

Ans. Circuit diagram present in black box is drawn in Fig. 14.98.

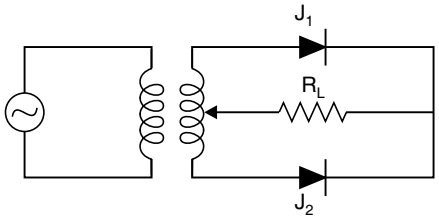


Fig. 14.98

It is full wave rectifier. For half cycle of the applied input a.c. one junction diode conducts and other does not conduct to work as half wave rectifier. Similarly for another half cycle the other junction diode conducts and the first one does not conduct to work is another half wave reacitifier, hence the complete applied a.c. input is rectified which is drawn across the load resistance R_L. The input and output waveform diagram is shown in the given figure 14.99

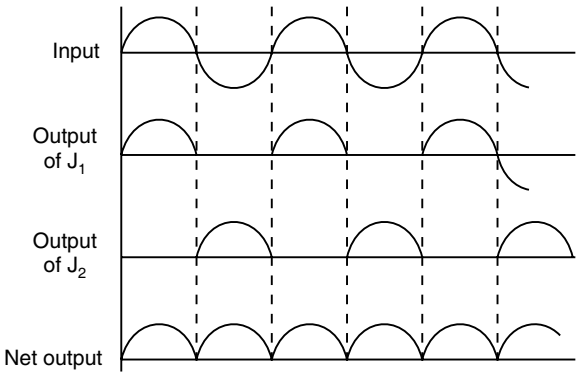


Fig. 14.99

MULTIPLE CHOICE QUESTIONS

1. The electrical conductivity of a semiconductor increases when electromagnetic radiation of wavelength shorter than 2480 nm is incident on it. The band gap (in eV) for the semi conductor is

(*a*) 0.9 (*b*) 0.7 (*c*) 0.5 (*d*) 1.1

2. The dominant mechanisms for motion of charge carriers in forward and reverse biased sillicon *p*-*n* junction are

(*a*) Drift in forward biased, diffusion in reverse bias.
(*b*) Diffusion in forward biased, drift in reverse bias.
(*c*) Diffusion in both forward and reverse bias
(*d*) Drift in both forward and reverse bias

3. Which of the following statement is not true?

(*a*) The resistance of intrinsic semiconductors decreases with increase of temperature
(*b*) Doping pure Si with trivalent impurities *p*-type semiconductors
(*c*) The majority carriers in *n*-type semiconductors are holes
(*d*) A *p*-*n* junction can act as a semiconductor diode.

4. For a BJT, the current amplification factor $\infty = 0.9$. This transistor is used in *CE* configuration. When the base current changes by 0.4 mA, the change in collector current will be

(*a*) 36 mA (*b*) 9 mA (*c*) 4 mA (*d*) 3.6 mA

5. A CE amplifier has a voltage gain 50, an input impedance of 100 ohm, and an output impedance of 200 ohm. The power gain of the amplifier will be

(*a*) 24 dB (*b*) 41 dB (*c*) 250 dB (*d*) 1250 dB

6. The input signal given to a *CE* amplifier having a voltage gain of 150 is $V_i = 200\ (15t + 10°)$. The corresponding output signal is

(*a*) $300 \cos (15t + 190°)$ (*b*) $300 \cos (15t + 90°)$
(*c*) $75 \cos (15t + 10°)$ (*d*) $2 \cos (15t + 90°)$

7. In a common base transistor circuit $I_C = 0.97$ mA, $I_b = 30\ \mu$A, then current gain, a =

(*a*) 0.97 (*b*) 0.097 (*c*) 95 (*d*) 500

8. In a middle of the depletion layer of a reverse biased *p-n* junction, the
(*a*) electric field is zero (*b*) potential is maximum
(*c*) electric field is maximum (*d*) potential is zero

9. For a transistor amplifier the voltage gain
(*a*) remains constant for all frequencies
(*b*) is high at high and low frequencies and constant in the middle frequency range
(*c*) is low at high and low frequencies and constant at mid frequencies
(*d*) none of the above

10. The peak voltage in the output of a half-wave diode rectifier fed with a sinusoidal signal without filter is 10 V. The d.c. component of the output voltage is
(*a*) $10/\sqrt{2}$ V (*b*) $10/\pi$ V (*c*) 10 V (*d*) $20/\pi$ V

11. The output of OR gate is 1
(*a*) if both the inputs are zero (*b*) if either or both inputs are 1
(*c*) only if both inputs are 1 (*d*) if either input zero

12. When an *npn* transistor is used as an amplifier
(*a*) electrons move froms base to collector
(*b*) holes move from emitter to base
(*c*) electrons move from collector to base
(*d*) holes move from base to emitter

13. In an *npn* transistor the collector current is 24 mA. If 80% of the electrons reach collector, its base current in mA is
(*a*) 36 (*b*) 26 (*c*) 16 (*d*) 6
(*e*) 3

14. Copper has face centred cubic (*fcc*) lattice with interatomic spacing equal to 2.54 Å. The value of the lattice constant for this lattice is
(*a*) 3.59 Å (*b*) 2.54 Å (*c*) 1.27 Å (*d*) 5.08 Å

15. The electrical conductivity of semiconductor increases when electromagnetic radiation of wavelength shorter than 2800 nm is incident on it. The band gap in (eV) for the semiconductor is
(*a*) 0.7 eV (*b*) 0.5 eV (*c*) 2.5 eV (*d*) 1.2 eV

Answers

1. (*c*)	**2.** (*b*)	**3.** (*c*)	**4.** (*d*)	**5.** (*b*)
6. (*a*)	**7.** (*a*)	**8.** (*a*)	**9.** (*c*)	**10.** (*b*)
11. (*b*)	**12.** (*a*)	**13.** (*d*)	**14.** (*a*)	**15.** (*b*).

TEST YOUR SKILLS

1. Draw the energy band diagram of a *p*-type semiconductor. Deduce an expression for the conductivity of a *p*-type semiconductor.

2. How is a *p*-type semiconductor formed? Name the major charge carriers in it. Draw the energy band diagram of a *p*-type semiconductor.

3. How does the energy gap in an intrinsic semiconductor vary when doped with a potential impurity?

4. Draw a circuit diagram to obtain the characteristics of a *p-n* transistor in common emitter configuration. Describe how you will obtain input and output characteristics. Give shape of the curves.
5. Draw the circuit diagram of a common emitter amplifier with appropriate biasing. What is the phase difference between the input and output signals? State two reasons why a common emitter amplifier is preferred to a common base amplifier.
6. Draw a circuit diagram of a common emitter amplier using *n-p-n* transistor. Show input and output voltages graphically.

   The current gain for common emitter amplifier is 59. If the emitter current is 6.0 mA, find (*i*) base current and (*ii*) collector current.
7. Draw a circuit diagram of a common base amplifier using *n-p-n* transistor. Show Input and output signals graphically.

   The current gain of a transistor in a common base arrangement is 0.95. Find the voltage gain and power gains, if the load resistance of output circuit is 400 kΩ and input resistance is 200 Ω.
8. If the base region of a transistor is made large as compared to a usual transistor, how does it affect; (*i*) the collector current "(*ii*) current gain of this transistor?

   What is the phase difference between the input and output signals of a common emitter amplier?
9. If the output of a 2-input NAND gate is fed as the input to a NOT gate (*i*) name the logic gate obtained and (*ii*) write down its truth table.
10. Draw the logic symbol of a 2-input NAND gate. Write down its truth table.
11. Draw the logic symbol of a 2-input NOR gate. Write down its truth table.
12. For the digital circuit given below write the truth table showing the outputs Y_1 ; Y_2 for all possible input at *A* and *B*.
13. Name the gate obtained from the combination of gates shown in the figure. Draw its logic symbol.
14. In the figure 14.100, circuit symbol of a logic gate and input waveform is shown (*i*) Name the logic gate, (*ii*) write its truth table and (*iii*) give the output wave form.
15. A semiconductor has equal electron and hole concentration of $2 \times 10^8/m^3$. On doping with a certain impurity, the hole concentration increases to $4 \times 10^{10}/m^3$.
    (*i*) What type of semiconductor is obtained on doping?
    (*ii*) Calculate the new electron concentration of the semiconductor.
    (*iii*) How does the energy gap vary with doping?
16. The figure 14.101 shows the *V-I* characteristics of a semiconducting device
    (*i*) Identify the semiconducing forward bias device used here,
    (*ii*) Draw the circuit diagram to obtain the given characteristics of this diode.
    (*iii*) Briefly explain how this device is used as a voltage regulator.

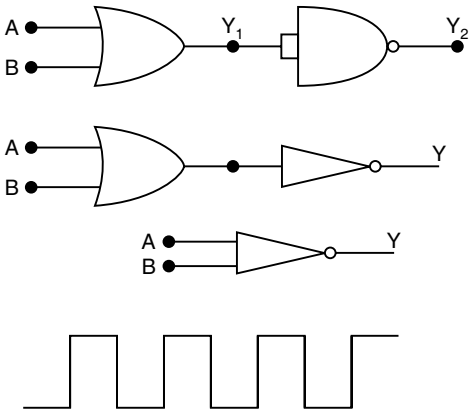


Fig. 14.100

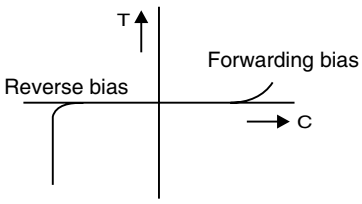


Fig. 14.101

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